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Vertical tunneling FET with Ge/Si doping-less heterojunction, a high-performance switch for digital applications

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A vertical tunneling field effect transistor composed of a doping-less tunneling heterojunction and an n⁺-drain is presented in this paper. Two highly-doped p⁺ silicon layers are devised to induce holes in an intrinsic source region. Due to employing a double gate configuration and Hafnium in the gate oxide, our proposed structure has an optimized electrostatic control over the channel. We have performed all the numerical simulations using Silvaco ATLAS, calibrated to the verified data of a device with the similar working principle. The impact of the wide range of non-idealities, such as trap-assisted tunneling, interface trap charges, and ambipolar conduction, is thoroughly investigated. We have also evaluated the impact of negative capacitance material to further improve our device switching characteristics. Introducing both n-channel and p-channel devices, and employing them into a 6T SRAM circuit, we have investigated its performance in terms of parameters like read and write SNM. The FOMs such as $I_{on} = 34.4$ μA/μm, $I_{on}/I_{off} = 7.17 \times 10^7$, and $f_T = 123$ GHz show that our proposed device is a notable candidate for both DC and RF applications.

Although conventional transistors with over barrier conduction mechanism are still the primary choice of nanoelectronics industry giants, the search for novel electronic devices with a different conduction mechanism and superior performance is continuously ongoing[1–3]. Tunneling field effect transistors (TFETs) are among most promising and successful alternatives[4,5]. They filter the high (low) energy electrons (holes) from the flowing charge carriers and form a tunneling energy window, theoretically leading to a very low off-state current[6]. The other advantage of such a filtering is that the subthreshold swing of tunneling FETs can beat the physically-limited subthreshold swing of MOSFETs. However, TFETs suffer from weaknesses such as low on-state current (I_{on})[7] and trap-related problems[8]. The low on-current issue has been addressed in several studies and solutions have been suggested[9–21]. On the other hand, employing the charge plasma technique seems to be a viable solution for trap-related problems in TFETs. Kumar and Janardhanan proposed the first charge plasma based TFET in which to induce holes in the source region Platinum with the work function of 5.93 eV was used[22]. Doping-less TFETs (DL-TFETs) based on InGaN[23] and heterojunction of GaAs$_{0.5}$Sb$_{0.5}$/In$_{0.53}$Ga$_{0.47}$As[24] are the other proposed DL-TFETs, which benefited from the special features of III–V materials and achieved the on-state current of 80.2 μA/μm and 40.5 μA/μm, respectively. Sharma et al.[25] suggested a DL-TFET with organic semiconductor, and obtained the I_{on} of 0.44 μA/μm and on/off current ratio (I_{on}/I_{off}) of 1.85×10^{11}. Using negative capacitance dielectric materials[26], 2D materials[27], L-shaped gate[28] and cladding layer concept[29,30] are the other proposed solutions for improving TFETs performance.

In the conventional doping-less TFETs, inductive metals have been employed to induce charge carriers in the source and drain regions. Such a technique increases the risk of silicide formation. In this article, we propose a TFET which benefits from a doping-less tunneling junction. Two highly-doped silicon layers are advised to induce holes in the intrinsic source region, while using n⁺-doped silicon as the drain region can reduce fabrication steps and challenges. Removing inductive metal over the drain region and employing a heavily doped drain can also lessen the gate-to-drain capacitance, leading to better AC performance. Here, using germanium in the source region is preferred over silicon due to its smaller band gap and higher electron mobility[31,32]. Considering the scalability, choosing a vertical structure is better than a horizontal one.

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Device configuration, fabrication process, and simulation procedure

Figure 1 depicts our proposed vertical TFET. It includes two cladding layers to induce holes in an intrinsic Ge source region, while to reduce the fabrication process complexity an n⁺ Si drain region is deposited at the top of the structure. The material of the channel region is silicon, too. Because of employing the n⁺ drain and the cladding layer in our doping-less tunneling junction device, we name it NCDL-TFET. The electrostatic integrity of the gate is enhanced by using a 2 nm layer of Hafnium as the gate oxide. All other design parameters are tabulated in Table 1.

Despite the complexity of fabrication process of nanoscale transistors, we suggest a fabrication process flow for realizing NCDL-TFET that, according to the literature[33,34], practically seems feasible. At the beginning a germanium layer is grown over a silicon substrate (see Fig. 2a,b). With the low-temperature in-situ doping technique, a p⁺ silicon layer, acting as a p-gate, is deposited over the germanium layer (see Fig. 2c). Then a thin isolator layer of SiO_2 is deposited over the silicon layer, following which a U-shaped trench is carved in the cladding layer (see Fig. 2d,e). In the next step, an intrinsic germanium layer is grown in this trench to act as the source region (see Fig. 2f). The layers of intrinsic and n⁺-doped silicon are deposited to form channel and drain regions, respectively (see Fig. 2g,h). After selective etching of the two above mentioned layers, the high-k gate oxide is deposited (see Fig. 2i). The gate metal is deposited, followed by the deposition of the SiO_2 as the spacer (see Fig. 2j,k). Finally, the source, gate, and drain contacts are connected (see Fig. 2l).

In Fig. 3, we have drawn the extracted I_D–V_G curve of Ref.[22] alongside the reproduced result of our device simulator, and it can be inferred that a good matching is obtained. Silvaco ATLAS device simulator was employed to assess our device performance[35]. We have used Shockley–Read–Hall (SRH) recombination model, CVT, fermi, and dynamic non-local band-to-band-tunneling (BTBT) models for all the simulations. The charge transport model of drift–diffusion is also activated. Due to the large indirect band gap of silicon and channel thickness of 10 nm quantum confinement model is not incorporated in the simulations. During the calibration process, $m_e = 0.22m_0$ and $m_h = 0.17m_0$ have been utilized.
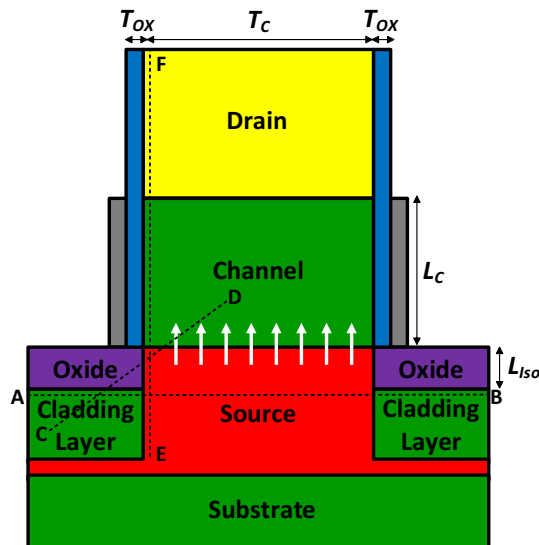

Figure 1. A schematic cross sectional view of vertical NCDL-TFET.

Parameter	Value
Gate oxide thickness (T_{ox})	2 nm
Channel length (L_C)	40 nm
Isolator length (L_{Iso})	3 nm
Channel thickness (T_C)	10 nm
Source/channel doping (N_{SC})	1×10^{15} cm⁻³
Drain doping (N_D)	3×10^{18} cm⁻³
Cladding layer doping (N_{Clad})	3×10^{19} cm⁻³
Gate metal work function (WF_G)	4.38 eV

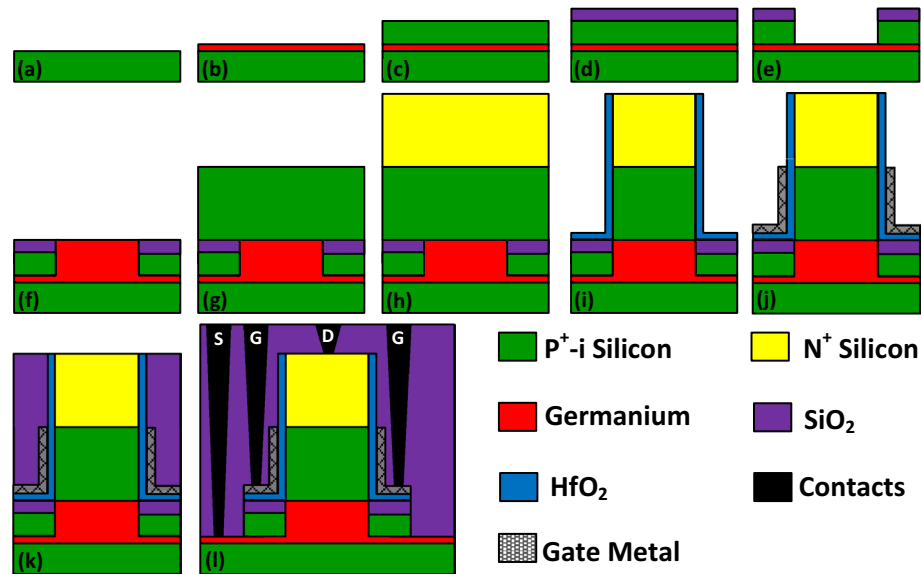**Table 1.** Default values of the proposed TFET parameters.

Figure 2. (**a–l**) Fabrication process steps of vertical NCDL-TFET structure.
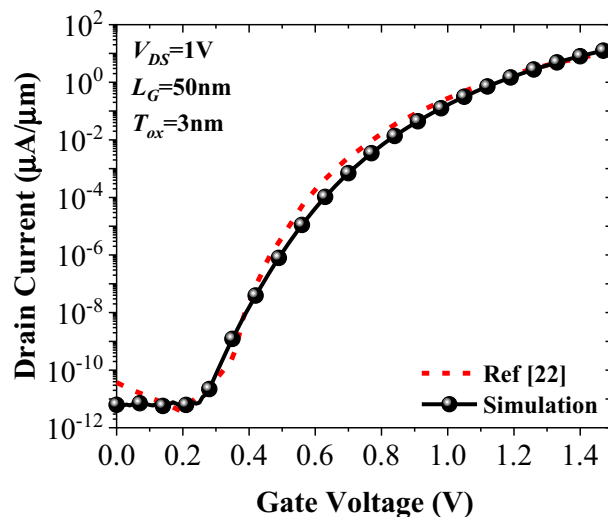

Figure 3. Comparison between the measured transfer characteristic of the doping-less TFET[22] and the reproduced curve by our calibrated simulation setup.

Simulation results

This section first evaluates the impact of cladding layers on the DC/RF performance of NCDL-TFET. Then, we assess our device performance in the presence of trap-assisted tunneling (TAT) and interface trap charges (ITC), temperature change, and ambipolar conduction. Then, we incorporate a negative capacitance in the design of NCDL-TFET, and its impact on our device performance is investigated. Finally, by designing a p-type doping-less TFET, a 6T SRAM cell is designed and its performance in terms of parameters such as reading and writing static noise margin (SNM) is evaluated.

Energy bands diagrams of NCDL-TFET along the A-B and C-D cutlines are depicted in Fig. 4a and b. As it can be inferred from Fig. 4a, no charge transport occurs between the cladding layers and the source region, mainly because of a large valence band offset between the mentioned regions. Figure 4b also depicts that no band-to-band tunneling happens in the parasitic tunneling path, which is from the valance band of the cladding layers to the conduction band of the channel. Thermionic emission is also suppressed due to the large band gap of SiO_2 and p⁺ doping of silicon layers. Figure 4c shows the energy bands profile of NCDL-TFET along the EF segment (as displayed in Fig. 1) in the off-state ($V_{GS} = 0$ V) for two different doping levels of the cladding layer. It can be seen that the higher doping of the cladding layers contributes to a smaller barrier width and a more-abrupt tunneling junction at the source-channel interface. This is mainly because increasing cladding layer doping levels induces more holes in the intrinsic source region. Figure 4d illustrates the energy bands diagram in the on-state
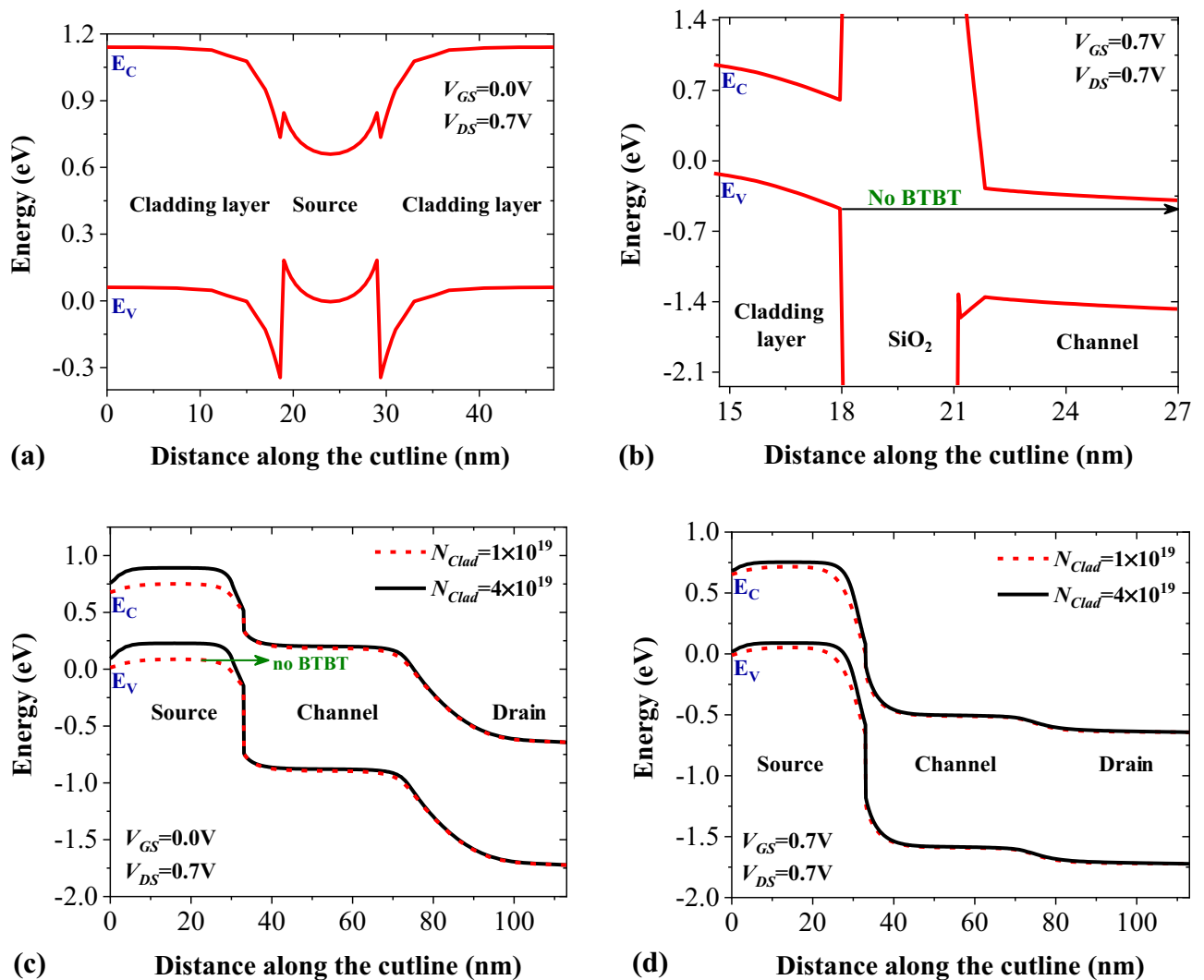
Figure 4. The energy bands diagram of NCDL-TFET along (**a**) A-B cutline and (**b**) C–D cutline. Impact of cladding layers doping concentration on the energy bands diagram of NCDL-TFET along the E–F cutline in (**c**) off-state and (**d**) on-state.

($V_{GS} = 0.7$ V), indicating that a more-favorable tunneling junction is obtained by using higher level of doping concentration in the cladding layers.

According to Fig. 5a, the band-to-band tunneling rate has almost a horizontally uniform profile across the channel. Such a uniformity facilitates having a higher on-state current. The tunneling charge carriers move toward the drain side of NCDL-TFET, as represented in Fig. 5b.

As discussed earlier, the doping density of cladding layers plays a significant role in the modulation of the energy bands profile at the source-channel junction of NCDL-TFET. In Fig. 6a, we have plotted the transfer characteristics of our device for four different values of N_{Clad}. It can be seen that the device with $N_{Clad} = 4 \times 10^{19}$ cm^{-3} has a better performance compared with that of its counterparts. In Fig. 6b, the impact of cladding layers doping concentration on the V_{off}, V_{th}, and I_{on} is evaluated. We have defined V_{off} as the gate voltage in which BTBT is triggered. For the calculation of V_{th}, we have employed the constant current method, as mentioned in[23]. Obviously, when $N_{Clad} = 4 \times 10^{19}$ cm^{-3} the device shows the best performance with minimum V_{off} and V_{th} and maximum I_{on} of 34.4 μA/μm. Transconductance, given by $g_m = \partial I_D / \partial V_{GS}$, is another important parameter for evaluating FETs' performance. From Fig. 6c, it can be inferred that increasing N_{Clad} results in higher g_m values, which are desirable for high-performance devices in low-noise, high-frequency applications. Another essential RF performance metric of a FET device is cut-off frequency (f_T). It is a function of transconductance and parasitic capacitances of the device. Figure 6d illustrates the impact of N_{Clad} on the f_T of NCDL-TFET. According to this figure, a significant frequency of 123 GHz can be achieved with $N_{Clad} = 4 \times 10^{19}$ illustrating that the role of higher g_m is more critical than increased parasitic capacitance. In Fig. 6e, we can see how the amount of N_{Clad} affects the transit time of charge carriers in NCDL-TFET. Transit time, which represents the time it takes for charge carriers to move from the source to the drain side, is inversely proportional to f_T, where $\tau = 1/(2\pi) \times f_T$ [36]. The results show that when
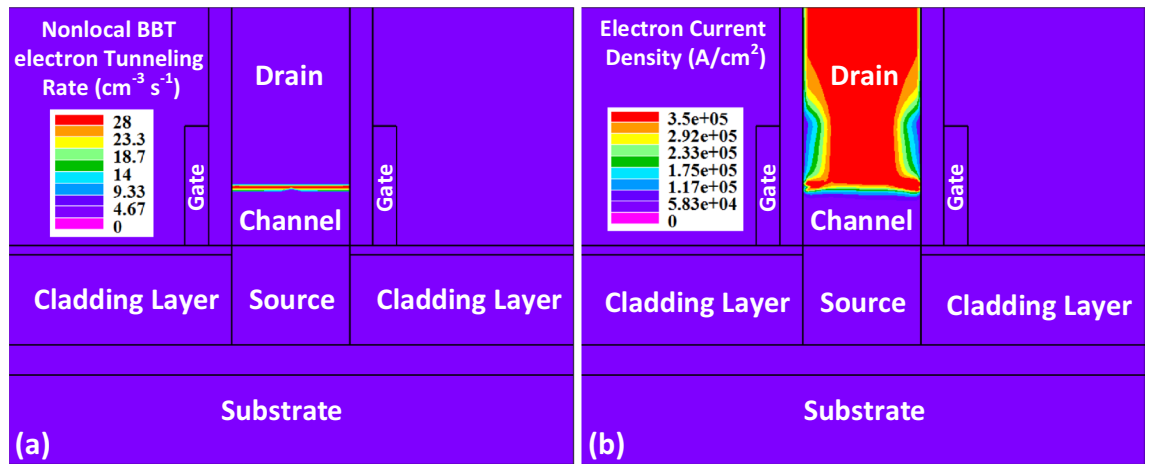
Figure 5. (**a**) Electron BTBT tunneling rate, and (**b**) electron current density contour maps at $V_{GS} = 0.7$ V and $V_{DS} = 0.7$ V.

N_{Clad} is at 4×10^{19}, the transit time values are the lowest, indicating that charge carriers require less time to move from the source to the drain side.

Figure 7a shows the impact of channel thickness on the transfer characteristics of NCDL-TFET. Increasing the channel thickness degrades the electrostatic control of the gate, contributing to higher off-state currents. We can see that tripling the channel thickness leads to an increment of I_{off} from 4.94×10^{-10} to 7.11×10^{-9} µA/µm. A slight reduction of on-state current with the increment of the channel thickness is also attributed to the electrostatic control degradation. However, the abovementioned values ensure us quantum confinement has no considerable impact on the on-state current of NCDL-TFET when $T_C = 10$ nm. In Fig. 7b, it is observable that with increasing T_C from 10 to 30 nm, the on/off ratio decreases from 6.96×10^{10} to 2.93×10^9. Moreover, minimum subthreshold swing with ~ 153% increase reaches from 18.42 to 28.24 mV/dec.

Defect at the heterojunctions and multi-phonon excitation at the oxide–semiconductor interface can adversely impact the performance of TFETs[8]. In Fig. 8a, we compare the impact of both non-idealities on the performance of our suggested device. In case (a), we have defined the trap energy (E_t) of 0.2 eV and the trap density (D_t) of 1×10^{12} cm^{-3} at the Ge-Si interface and the interface trap density (D_{it}) of 3×10^{12} cm^{-2} eV^{-1} at the HfO$_2$-Si interface[37], while in case (b), a hetero-oxide interface (comprising of 0.5 nm SiO$_2$ and 1.5 nm HfO$_2$) has been employed. So, the $D_{it} = 3 \times 10^{11}$ cm^{-2} eV^{-1} was used in the INTERFACE model of the device simulator. The change in the subthreshold swing of NCDL-TFET at the presence of these detrimental effects is shown in the inset of the figure. Figure 8b illustrates that by including both TAT and ITC models I_{off} with almost three decades increment reaches to 4.88×10^{-7} µA/µm, leading to nearly three decades reduction of the on/off currents ratio from 6.96×10^{10} to 7.17×10^7. On the other hand, employing a hetero-oxide interface improves the off-state current and the on/off currents ratio. However, it leads to a more complicated fabrication process.

The impact of temperature variation on our NCDL-TFET performance is investigated in Fig. 9a, where we have used temperatures ranging from 300 to 400 K. Since thermal generation of charge carriers plays a significant role in subthreshold conductance, the temperature's impact on the off-state current is more significant than that on the on-state current. However, the $I_{off} = 3.65 \times 10^{-7}$ µA/µm shows that NCDL-TFET has lower power dissipation than the short channel MOSFET even at temp = 400 K. In contrast, the on-state current remains almost unchanged, mainly because the transmission probability equation defined in Ref.[4] has no direct dependency on the temperature. The inset of Fig. 9a shows that with an 100 K increment of temperature, the SS_{min} increases from 18.42 to 30.51 mV/dec which is still significantly lower than subthreshold swing of MOSFETs.

In order to suppress ambipolar conduction in the proposed device, the drain region of the device has not been heavily doped. As depicted in Fig. 9b, by choosing $N_D = 3 \times 10^{18}$ cm^{-3}, the ambipolar current (I_{amb}) is even lower than the off-state current. By one order of magnitude increase in N_D the ambipolarity of NCDL-TFET rises about seven decades. As a result, the I_{on}/I_{amb} ratio reaches from 1.29×10^{13} to 1.25×10^6, exhibiting dramatic reduction of our device reliability.

Comparing the achieved performance of our proposed device with some of the recently published works on the same topic, listed in Table 2, indicates that NCDL-TFET is a notable candidate for CMOS applications.

Paraelectric Hafnium, a CMOS-compatible material, has a high potential to act as a negative capacitance material. Adding materials such as Si[38], Al[39], and ZrO$_2$[40] into paraelectric HfO$_2$ can be a viable solution to attain ferroelectricity. We have employed yttrium-doped HfO$_2$ (Y: HfO$_2$) in a Metal-ferroelectric-insulator-semiconductor (MFIS) configuration to enhance our device switching performance, as illustrated in Fig. 10. To evaluate the impact of Y: HfO$_2$ material on the performance of NCDL-TFET, we first calibrated our device simulator with the extracted polarization curve of[41] (see Fig. 11a). Then, the on-state current is calculated using the procedure explained in our previous work[42]. Figure 11b shows the impact of the thickness of (Y: HfO$_2$) on the I_D-V_G curve of our proposed structure. It should be noted that although increasing T_{fe} improves the subthreshold swing, it can lead to more considerable hysteresis, which is not a desirable in CMOS applications. The inset shows the extracted values of V_{th} and SS_{avg}, and it can be inferred that the higher values of T_{fe} lower V_{th} and improve SS_{avg}.
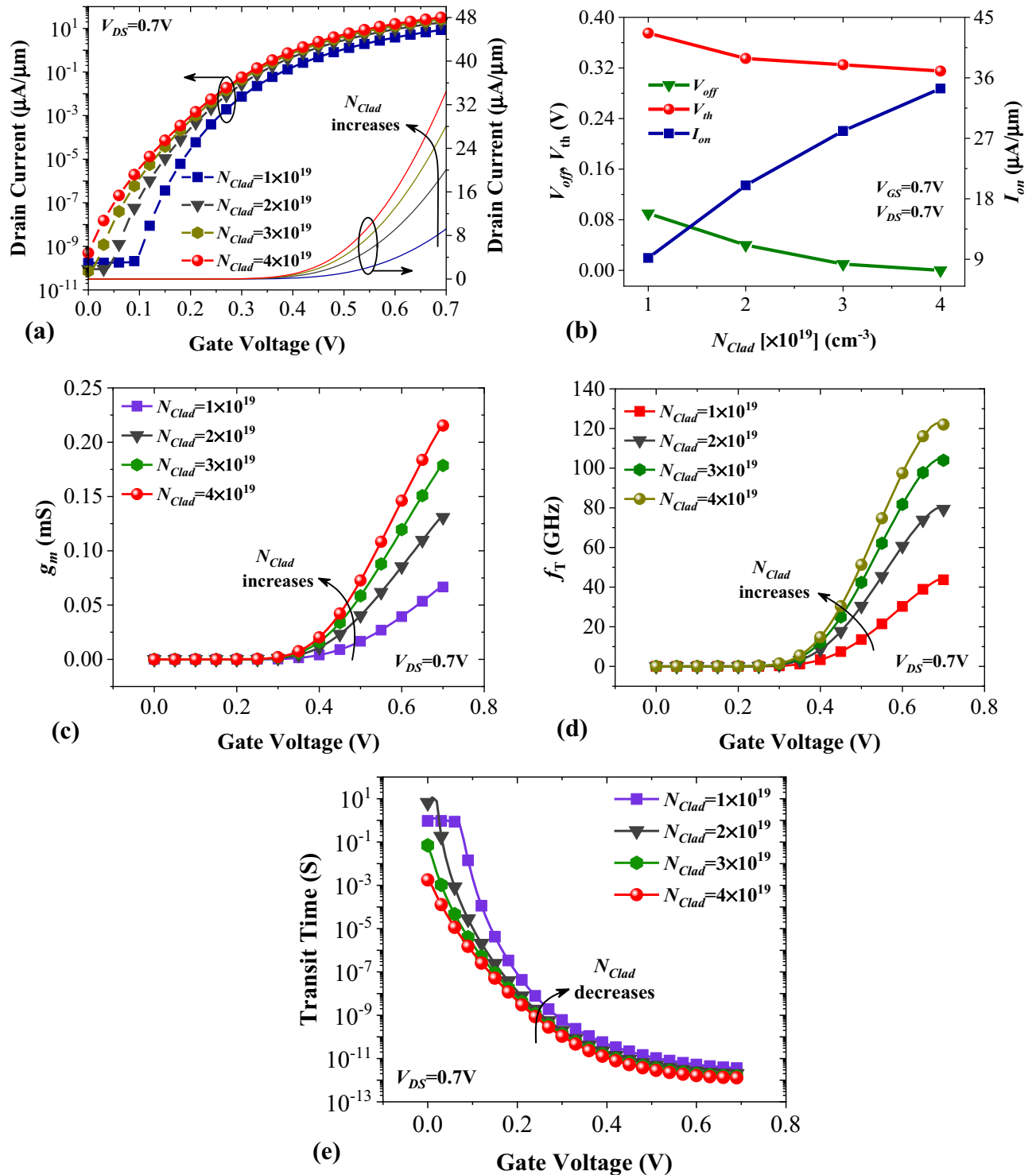
Figure 6. Impact of cladding layers doping concentration on (**a**) transfer characteristic, (**b**) V_{th}, V_{off}, and I_{on}, (**c**) transconductance, (**d**) cut-off frequency and (**e**) transit time of vertical NCDL-TFET.

A more pragmatic assessment of a device's performance can be achieved by incorporating it into a familiar circuit configuration. In pursuit of this objective, our attention shifts to a hybrid six-transistor (6T) SRAM cell, depicted in Fig. 12. This configuration comprises four n-channel and two p-channel devices. The p-channel device chosen is a vertical PDL-TFET, designed along the same principles as the NCDL-TFET. According to the device structure exhibited in Fig. 13a, PDL-TFET has an intrinsic silicon source located at the bottom of the transistor, while germanium is employed in the channel and drain regions. All pertinent dimensions, parameter values, and activated models for simulations remain consistent with those utilized in NCDL-TFET simulations, with the exception of gate and source work functions which are assigned values of 4.65 eV and 3.9 eV, respectively. In Fig. 13b, our device simulator's accuracy is validated against simulation outcomes from the device highlighted
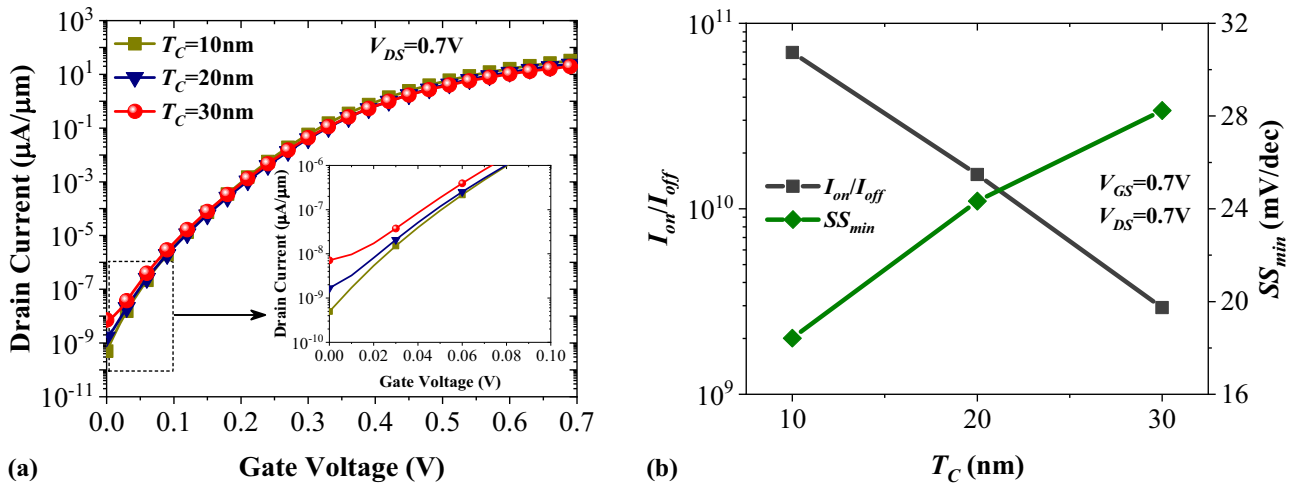
Figure 7. Impact of channel thickness on (**a**) transfer characteristic, and (**b**) I_{on}/I_{off}, and SS_{min} of vertical NCDL-TFET.
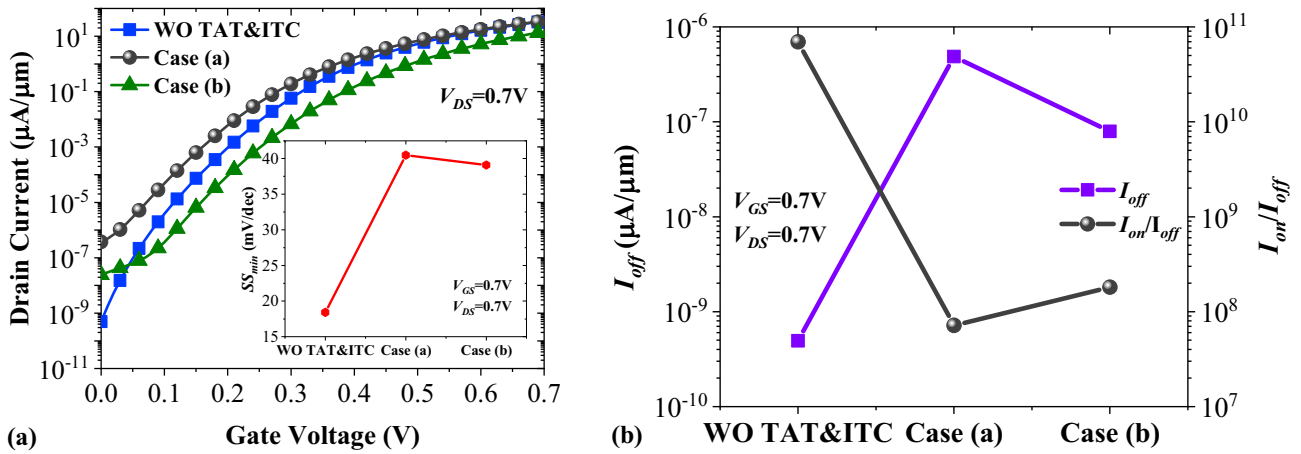

Figure 8. Impact of trap-assisted tunneling and interface trap charges on (**a**) transfer characteristic and (**b**) I_{off} and I_{on}/I_{off} of vertical NCDL-TFET.
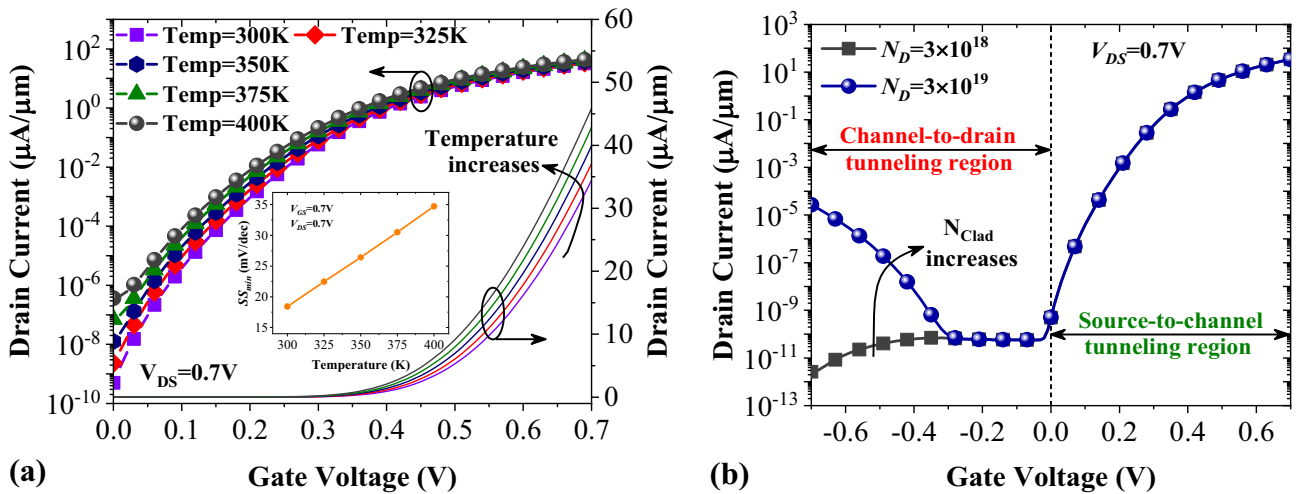

Figure 9. (**a**) Impact of temperature variation and (**b**) impact of drain doping concentration on the transfer characteristic of vertical NCDL-TFET.

References	Material	I_{on} (μA/μm)	SS_{avg} (mV/dec)	I_{on}/I_{off}	f_T (GHz)	V_{Bias} (V)	QC	ITC	TAT
[22]	Si	11	~ 100	1.1×10^{12}	–	1.5	✗	✗	✗
[23]	InGaN	80.2	7.9	8.02×10^{13}	119	0.5	✗	✗	✓
[24]	$GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$	40.5	20.3	4.86×10^9	~75	0.6	✗	✓	✗
[25]	$CH_3NH_3PbI_3$	0.44	27.33	1.85×10^{11}	268	1	✓	✗	✓
[26]	Negative Cap-Si	~ 36	~ 65	$\sim 10^{11}$	–	1.2	✗	✗	✓
[27]	WTe_2	222	54.15	2.22×10^5	–	0.5	Atomistic simulation		
[28]	Si	10	40	$\sim 10^{12}$	4.5	1	✗	✗	✓
[29]	Ge-Si	27.28	42.43	8.24×10^8	89.31	0.7	✗	✓	✓
		4.07	40.26	1.2×10^{10}			✓	✗	✓
[30]	Ge-Si	7.57	18.65	1.48×10^8	–	1	✓	✓	✓
This work	Ge-Si	34.4	51.78	7.17×10^7	123	0.7	✗	✓	✓

Table 2. Switching performance comparison of some recently introduced doping-less TFETs.
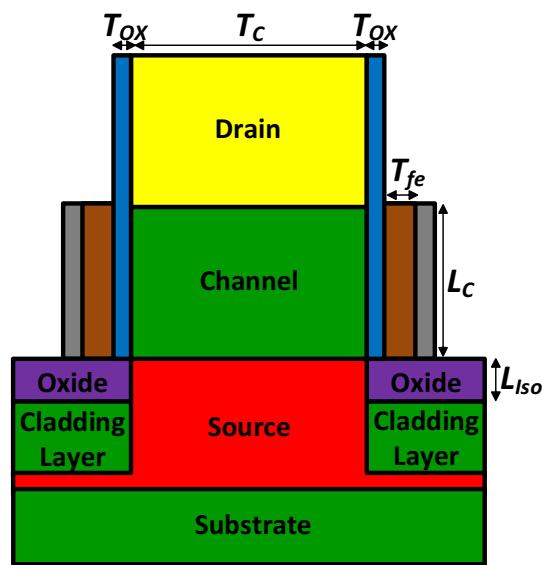

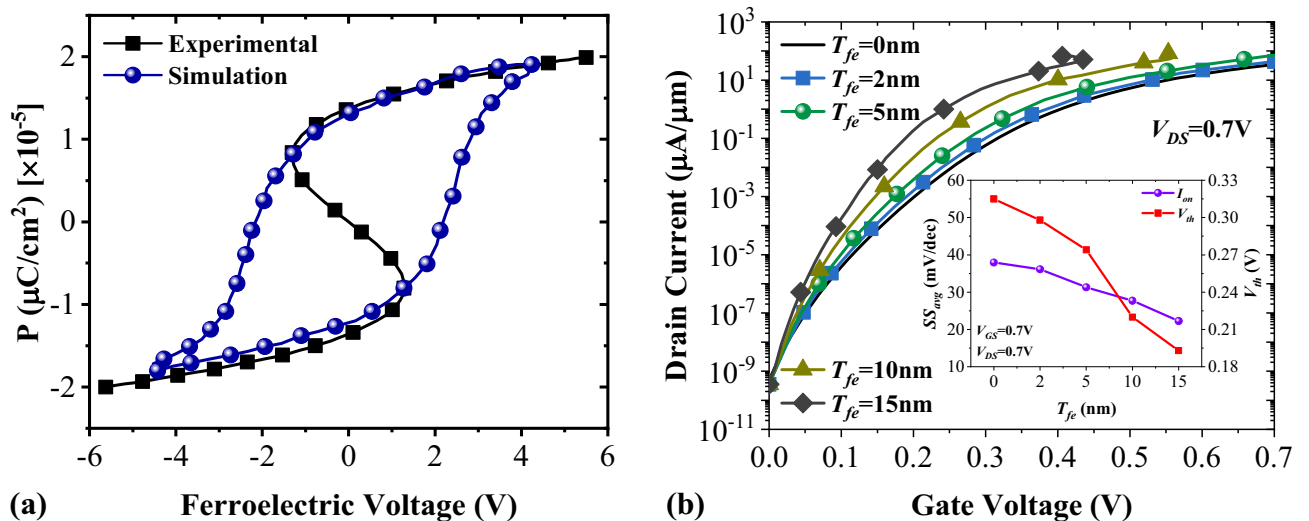**Figure 10.** A schematic cross sectional view of a negative capacitance-based vertical NCDL-TFET.

Figure 11. (**a**) Calibration of the p–v curve using experimental data from Ref.[41] and (**b**) the impact of thickness of ferroelectric material on the transfer characteristics of NCDL-TFET.
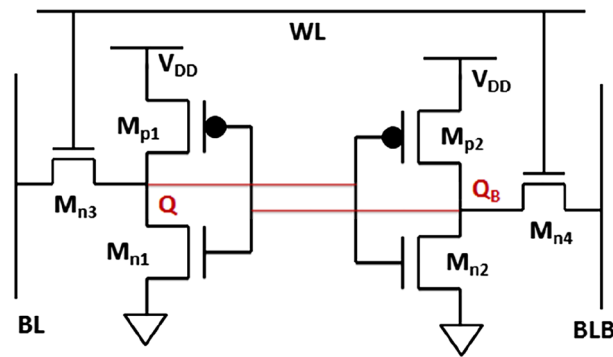
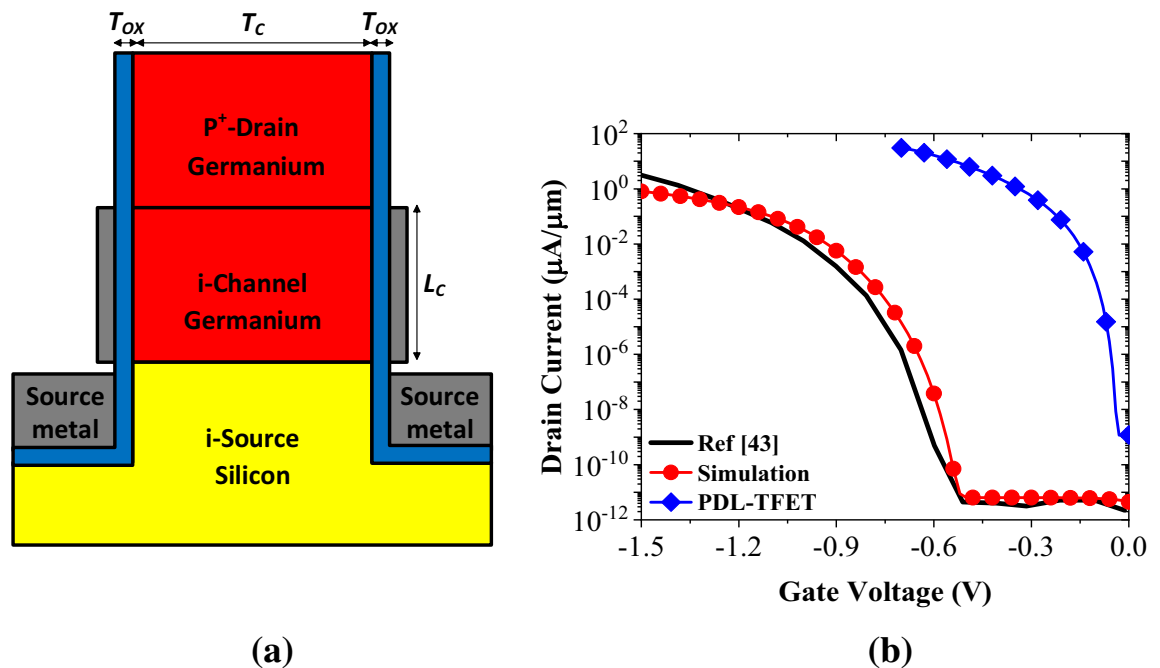**Figure 12.** Schematic of a 6T SRAM cell.

(a)

(b)

Figure 13. (**a**) A schematic cross sectional view of vertical PDL-TFET and (**b**) comparison between the measured transfer characteristic of the doping-less P-TFET of[43] and the reproduced curve by our calibrated simulation setup. The transfer characteristic of vertical PDL-TFET is also plotted in the figure.

in Ref.[43]. Additionally, we have plotted the transfer characteristics of PDL-TFET, which shows more-optimum performance for low-power applications.

By incorporating both n-channel and p-channel devices, we construct the 6T hybrid SRAM cell using four NCDL-TFET devices (M_{n1}, M_{n2}, M_{n3}, and M_{n4}) along with two PDL-TFET devices (M_{p1} and M_{p2}). The stability performance of the 6T hybrid SRAM cell is explored through the examination of different static noise margins (SNMs) and their alterations in response to varying supply voltages (V_{DD}). To ascertain the SRAM cell's SNM, the voltage transfer characteristics (VTC) of the two cross-coupled inverters are plotted. Various SNM values can be derived as the cell functions in the HOLD, READ, and WRITE modes. When the cell is in a HOLD or data retention state, the word line (WL) remains inactive, ensuring that the access transistors remain off. In this state, the cell retains its data using the cross-coupled inverters. Figure 14a visually presents the properties of the HOLD SNM and their shifts corresponding to different supply voltages (V_{DD}). Notably, the HOLD SNM diminishes proportionally as the supply voltage decreases[44].

During the READ operation, the SRAM cell is highly susceptible to noise[45]. Following a READ action, the cell must preserve its state without erasing the stored value. Bit lines (BL and BLB) are prepared for the READ operation prior to activating the word line (WL). The READ SNM of the SRAM cell, observed across various supply voltages, is illustrated in Fig. 14b. The minimal bit line voltage required to alter the cell's state is referred to as the WRITE margin. During the WRITE operation, data bits are transmitted on BL and BLB before enabling the word line. The WRITE action's properties in terms of SNM are portrayed in Fig. 14c. A summary of the HOLD,
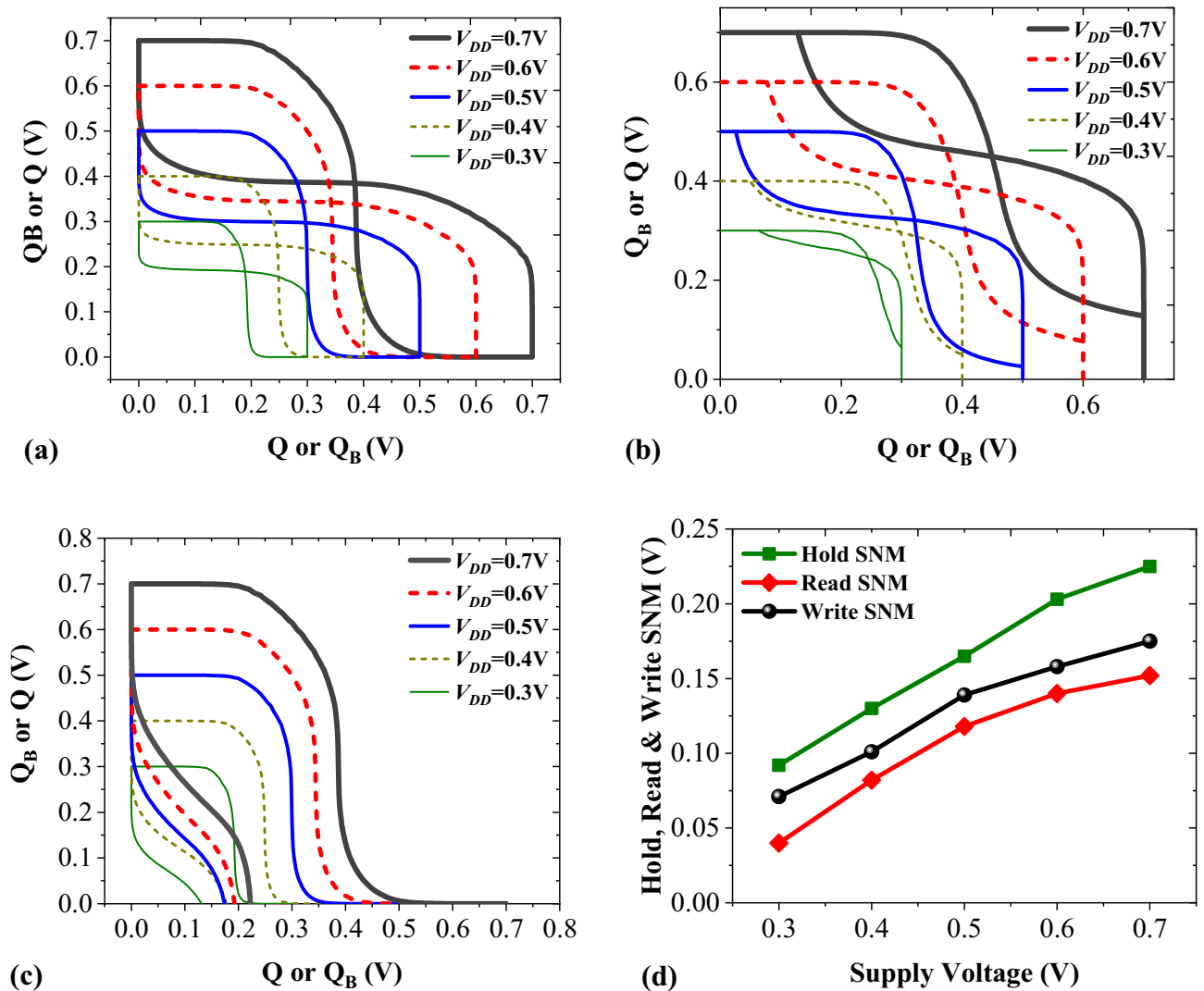
Figure 14. (**a**) Hold (**b**) Read and (**c**) Write SNM of 6T hybrid SRAM cell for different supply voltages. (**d**) Summary of Hold, Read and Write SNM for different supply voltages (V_{DD}).

READ, and WRITE noise margins for different supply voltages is presented in Fig. 14d. Across all scenarios, the noise margin decreases with diminishing supply voltage, rendering the SRAM cell increasingly unstable.

Conclusion

We have suggested a TFET composed of a doping-less tunneling heterojunction and an n$^+$-drain region in a vertical configuration. Due to using heterojunction of germanium/silicon in the tunneling interface, the on-state performance of our proposed device is more robust than Si-based doping-less TFETs. By employing a virtual fabrication process, we have shown that our structure can be realized in a feasible and convenient manner. Using Silvaco ATLAS, we have assessed the effect of non-idealities, such as defects at the tunneling interface and temperature, on our device performance. Our proposed device offers high scalability, sub-60 mV/dec performance even in the presence of defects, and higher AC performance than conventional doping-less TFETs. Although, using n$^+$ doping in the drain region can increase the thermal budget but effectively reduce gate-to-drain parasitic capacitance and reduce fabrication steps. Moreover, silicide formation is no longer a challenge due to using highly doped cladding layers instead of inductive metal. We have also utilized yttrium-doped Hafnium as a negative capacitance material in an MFIS configuration, and a considerable improvement without any hysteresis was obtained. A CMOS-compatible p-TFET was also designed to meet all the requirements for developing a SRAM cell. The parameters such as I_{on} = 34.4 μA/μm, SS_{avg} = 51.78 mV/dec, and f_T = 123 GHz illustrate that NCDL-TFET is a notable candidate for high-performance applications such as designing SRAMs with lower power dissipation.

Data availability

The datasets used and/or analyzed during the current study available from the corresponding author on reasonable request.

References

1. Gopalakrishnan, K., Griffin, P. B. & Plummer, J. D. Impact ionization MOS (I-MOS)-Part I: Device and circuit simulations. *IEEE Trans. Electron Devices* **52**, 69–76. https://doi.org/10.1109/TED.2004.841344 (2004).
2. Salahuddin, S. & Datta, S. Use of negative capacitance to provide voltage amplification for low power nanoscale devices. *Nano Lett.* **8**, 405–410. https://doi.org/10.1021/nl071804g (2008).
3. Niroui, F. *et al.* Tunneling nanoelectromechanical switches based on compressible molecular thin films. *ACS Nano* **9**, 7886–7894. https://doi.org/10.1021/acsnano.5b02476 (2015).
4. Ionescu, A. M. & Riel, H. Tunnel field-effect transistors as energy-efficient electronic switches. *Nature* **479**, 329–337. https://doi.org/10.1038/nature10679 (2011).
5. Seabaugh, A. C. & Zhang, Q. Low-voltage tunnel transistors for beyond CMOS logic. *Proc. IEEE* **98**, 2095–2110. https://doi.org/10.1109/JPROC.2010.2070470 (2010).
6. Knoch, J., Mantl, S. & Appenzeller, J. Impact of the dimensionality on the performance of tunneling FETs: Bulk versus one-dimensional devices. *Solid State Electron.* **51**, 572–578. https://doi.org/10.1016/j.sse.2007.02.001 (2007).
7. Avci, U. E., Morris, D. H. & Young, I. A. Tunnel field-effect transistors: Prospects and challenges. *IEEE J. Electron Devices Soc.* **3**, 88–95. https://doi.org/10.1109/JEDS.2015.2390591 (2015).
8. Sant, S., Schenk, A., Moselund, K. & Riel, H. in *2016 74th Annual Device Research Conference (DRC)* 1–2 (IEEE, 2016), https://doi.org/10.1109/DRC.2016.7548413.
9. Cherik, I. C. & Mohammadi, S. Cylindrical electron–hole bilayer TFET with a single surrounding gate and induced quantum confinement. *J. Comput. Electron.* **21**, 235–242. https://doi.org/10.1007/s10825-021-01849-7 (2022).
10. Kato, K., Matsui, H., Tabata, H., Takenaka, M. & Takagi, S. Bilayer tunneling field effect transistor with oxide-semiconductor and group-IV semiconductor hetero junction: Simulation analysis of electrical characteristics. *AIP Adv.* **9**, 055001. https://doi.org/10.1063/1.5088890 (2019).
11. Padilla, J. L., Medina-Bailon, C., Alper, C., Gamiz, F. & Ionescu, A. M. Confinement-induced InAs/GaSb heterojunction electron–hole bilayer tunneling field-effect transistor. *Appl. Phys. Lett.* **112**, 182101. https://doi.org/10.1063/1.5012948 (2018).
12. Dewey, G. *et al.* in *2011 International Electron Devices Meeting* 33–36 (IEEE, 2011), https://doi.org/10.1109/IEDM.2011.6131666.
13. Mohata, D. *et al.* Experimental staggered-source and N+ pocket-doped channel III–V tunnel field-effect transistors and their scalabilities. *Appl. Phys. Express* **4**, 024105. https://doi.org/10.1143/APEX.4.024105 (2011).
14. Mookerjea, S. *et al.* in *2009 IEEE International Electron Devices Meeting (IEDM)* 1–3 (IEEE, 2009), https://doi.org/10.1109/IEDM.2009.5424355.
15. Shih, P.-C., Hou, W.-C. & Li, J.-Y. A U-gate InGaAs/GaAsSb heterojunction TFET of tunneling normal to the gate with separate control over ON-and OFF-state current. *IEEE Electron Device Lett.* **38**, 1751–1754. https://doi.org/10.1109/LED.2017.2759303 (2017).
16. Hanna, A. & Hussain, M. M. Si/Ge hetero-structure nanotube tunnel field effect transistor. *J. Appl. Phys.* **117**, 014310. https://doi.org/10.1063/1.4905423 (2015).
17. Cherik, I. C. & Mohammadi, S. Double quantum-well nanotube tunneling field-effect transistor. *Mater. Sci. Semicond. Process.* **142**, 106514. https://doi.org/10.1016/j.mssp.2022.106514 (2022).
18. Cherik, I. C., Mohammadi, S. & Orouji, A. A. Switching performance enhancement in nanotube double-gate tunneling field-effect transistor with Germanium source regions *IEEE Trans. Electron Devices* https://doi.org/10.1109/TED.2021.3124984 (2021).
19. Musalgaonkar, G., Sahay, S., Saxena, R. S. & Kumar, M. J. Nanotube tunneling fet with a core source for ultrasteep subthreshold swing: A simulation study. *IEEE Trans. Electron Devices* **66**, 4425–4432. https://doi.org/10.1109/TED.2019.2933756 (2019).
20. Tripathy, M. R. *et al.* Device and circuit-level assessment of GaSb/Si heterojunction vertical tunnel-FET for low-power applications. *IEEE Trans. Electron Devices* **67**, 1285–1292. https://doi.org/10.1109/TED.2020.2964428 (2020).
21. Lee, H., Park, J.-D. & Shin, C. Performance booster for vertical tunnel field-effect transistor: Field-enhanced high-κ layer. *IEEE Electron Device Lett.* **37**, 1383–1386. https://doi.org/10.1109/LED.2016.2606660 (2016).
22. Kumar, M. J. & Janardhanan, S. Doping-less tunnel field effect transistor: Design and investigation. *IEEE Trans. Electron Devices* **60**, 3285–3290. https://doi.org/10.1109/TED.2013.2276888 (2013).
23. Duan, X. *et al.* A high-performance gate engineered InGaN dopingless tunnel FET. *IEEE Trans. Electron Devices* **65**, 1223–1229. https://doi.org/10.1109/TED.2018.2796848 (2018).
24. Bhattacharyya, A., Chanda, M. & De, D. GaAs$_{0.5}$Sb$_{0.5}$/In$_{0.53}$Ga$_{0.47}$As heterojunction dopingless charge plasma-based tunnel FET for analog/digital performance improvement. *Superlattices Microstruct.* **142**, 106522. https://doi.org/10.1016/j.spmi.2020.106522 (2020).
25. Sharma, P., Madan, J., Pandey, R. & Sharma, R. Numerical simulations of a novel CH$_3$NH$_3$PbI$_3$ based double-gate dopingless tunnel FET. *Semicond. Sci. Technol.* **36**, 055008. https://doi.org/10.1088/1361-6641/abec13 (2021).
26. Lahgere, A., Panchore, M. & Singh, J. Dopingless ferroelectric tunnel FET architecture for the improvement of performance of dopingless n-channel tunnel FETs. *Superlattices Microstruct.* **96**, 16–25. https://doi.org/10.1016/j.spmi.2016.05.004 (2016).
27. Dubey, P. K. & Kaushik, B. K. A charge plasma-based monolayer transition metal dichalcogenide tunnel FET. *IEEE Trans. Electron Devices* **66**, 2837–2843. https://doi.org/10.1109/TED.2019.2909182 (2019).
28. Li, C. *et al.* A novel gate engineered L-shaped dopingless tunnel field-effect transistor. *Appl. Phys. A Mater. Sci. Process.* **126**, 412. https://doi.org/10.1007/s00339-020-03554-x (2020).
29. Cherik, I. C. & Mohammadi, S. Vertical cladding layer-based doping-less tunneling field effect transistor: A novel low-power high-performance device. *IEEE Trans. Electron Devices* https://doi.org/10.1109/TED.2021.3138669 (2022).
30. Cherik, I. C. & Mohammadi, S. Design insights into switching performance of germanium source L-shaped gate dopingless TFET based on cladding layer concept. *IEEE Trans. Electron Devices* https://doi.org/10.1109/TED.2022.3229257 (2022).
31. Kim, S. H. *et al.* Tunnel field effect transistor with raised germanium source. *IEEE Electron Device Lett.* **31**, 1107–1109. https://doi.org/10.1109/LED.2010.2061214 (2010).
32. Toh, E.-H., Wang, G. H., Samudra, G. & Yeo, Y.-C. Device physics and design of germanium tunneling field-effect transistor with source and drain engineering for low power and high performance applications. *J. Appl. Phys.* **103**, 104504. https://doi.org/10.1063/1.2924413 (2008).
33. Chen, S. *et al.* Symmetric U-shaped gate tunnel field-effect transistor. *IEEE Trans. Electron Devices* **64**, 1343–1349. https://doi.org/10.1109/TED.2017.2647809 (2017).
34. Bagga, N., Kumar, A. & Dasgupta, S. Demonstration of a novel two source region tunnel FET. *IEEE Trans. Electron Devices* **64**, 5256–5262. https://doi.org/10.1109/TED.2017.2759898 (2017).
35. Silvaco, ATLAS Device Simulation Software User's Manual, No. Version 3.2. 2015.
36. Imenabadi, R. M., Saremi, M. & Vandenberghe, W. G. A novel PNPN-like Z-shaped tunnel field-effect transistor with improved ambipolar behavior and RF performance. *IEEE Trans. Electron Devices* **64**, 4752–4758. https://doi.org/10.1109/TED.2017.2755507 (2017).

37. Kim, S. W., Kim, J. H., Liu, T.-J.K., Choi, W. Y. & Park, B.-G. Demonstration of L-shaped tunnel field-effect transistors. *IEEE Trans. Electron Devices* **63**, 1774–1778. https://doi.org/10.1109/TED.2015.2472496 (2015).
38. Lomenzo, P. D. *et al.* Ferroelectric phenomena in Si-doped HfO2 thin films with TiN and Ir electrodes. *J. Vac. Sci. Technol. B Nanotechnol. Microelectron. Mater. Process. Meas. Phenom.* **32**, 03D123. https://doi.org/10.1116/1.4873323 (2014).
39. Mueller, S. *et al.* Incipient ferroelectricity in Al-doped HfO$_2$ thin films. *Adv. Funct. Mater.* **22**, 2412–2417. https://doi.org/10.1002/adfm.201103119 (2012).
40. Lee, M. *et al.* in *2015 IEEE International Electron Devices Meeting (IEDM).* 22–25 (IEEE, 2015), https://doi.org/10.1109/IEDM.2015.7409759.
41. Müller, J. *et al.* Ferroelectricity in yttrium-doped hafnium oxide. *J. Appl. Phys.* **110**, 114113. https://doi.org/10.1063/1.3667205 (2011).
42. Cherik, I. C., Abbasi, A., Maity, S. K. & Mohammadi, S. Junctionless tunnel field-effect transistor with a modified auxiliary gate, a novel candidate for high-frequency applications. *Micro Nanostruct* **174**, 207477. https://doi.org/10.1016/j.micrna.2022.207477 (2022).
43. Bashir, F. & Loan, S.A. in *2014 IEEE 2nd International Conference on Emerging Electronics (ICEE)* 1–4 (IEEE, 2014), https://doi.org/10.1109/ICEmElec.2014.7151160.
44. Seevinck, E., List, F. J. & Lohstroh, J. Static-noise margin analysis of MOS SRAM cells. *IEEE J. Solid-State Circuits* **22**, 748–754. https://doi.org/10.1109/JSSC.1987.1052809 (1987).
45. Grossar, E., Stucchi, M., Maex, K. & Dehaene, W. Read stability and write-ability analysis of SRAM cells for nanometer technologies. *IEEE J. Solid-State Circuits* **41**, 2577–2588. https://doi.org/10.1109/JSSC.2006.883344 (2006).

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Competing interests

The authors declare no competing interests.

Additional information

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