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Electrical and dielectric parameters in TiO_2-NW/Ge-NW heterostructure MOS device synthesized by glancing angle deposition technique

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This paper reports the catalyst-free coaxial TiO_2/Ge-nanowire (NW) heterostructure synthesis using the glancing angle deposition (GLAD) technique integrated into an electron beam evaporator. The frequency and voltage dependence of the capacitance–voltage (C–V) and conductance–voltage (G/ω–V) characteristics of an Ag/TiO_2-NW/Ge-NW/Si device over a wide range of frequency (10 kHz–5 MHz) and voltage (− 5 V to + 5 V) at room temperature were investigated. The study established strong dependence on the applied frequency and voltage bias. Both C–V and G/ω–V values showed wide dispersion in depletion region due to interface defect states (D_{it}) and series resistance (R_s). The C and G/ω value decreases with an increase in applied frequency. The voltage and frequency-dependent D_{it} and R_s were calculated from the Hill-Coleman and Nicollian–Brews methods, respectively. It is observed that the overall D_{it} and R_s for the device decrease with an increase in the frequency at different voltages. The dielectric properties such as dielectric constant (ϵ′), loss (ϵ″) and loss tangent (tan δ) were determined from the C–V and G/ω–V measurements. It is observed that ϵ′, ϵ″ decreases with the increase in frequency. Therefore, the proposed MOS structure provides a promising alternative approach to enhance the device capability in the opto-electronics industry.

One-dimensional (1D) nanostructures like nanowires and nanorods have attracted huge interest over the last few decades in the field of metal oxide semiconductor (MOS) for various applications like photodetectors[1–6], sensors[7,8], photovoltaic systems[9], non-volatile memory applications[10,11] etc. Following the Moore's law, the current semiconductor based MOS devices are facing a technological limitation in the form of scalability and leakage current. In order to further improve the MOS device performance, the International Technology Roadmap for semiconductors (ITRS) for future technology has recommended the use of a high mobility material as an alternative solution. In this context, recent papers have reported Germanium (Ge) with high-k dielectric based MOS devices which show good overall performance[12,13]. This is because Ge has high electron and hole mobility compared to silicon (Si) and a low band gap which enables operation at low voltage[14]. This feature, together with the opportunity to co-integrate Ge with high-k dielectrics such as Al_2O_3, HfO_2, TiO_2 etc., makes Ge a practical candidate for future MOS device applications. However, the integration of Ge with a MOS capacitor is challenging due to the native unintentional formation of GeO_x which is unstable compared to SiO_2. This issue is mitigated by the integration of titanium dioxide (TiO_2) which is a high dielectric material with Ge. The unstable GeO_x is reduced by the diffusion of Ge into the TiO_2. At the same time, rutile-TiO_2 can be formed which has a high-dielectric constant[15]. Recent reports suggests that this approach can be achieved by various synthesis techniques for different applications[16–18]. Amongst these synthesis techniques, the glancing angle deposition (GLAD) is a catalyst free environment friendly technique which can synthesize numerous materials for various applications[2,19–21]. Furthermore, vertical nanowires can be easily achieved with the GLAD technique compared to other available techniques[22].

In this work, a Ag/TiO_2-NW/Ge-NW/Si (MOS) device is synthesized using the GLAD technique integrated into an electron-beam evaporator. The frequency and voltage dependence capacitance (C) and conductance

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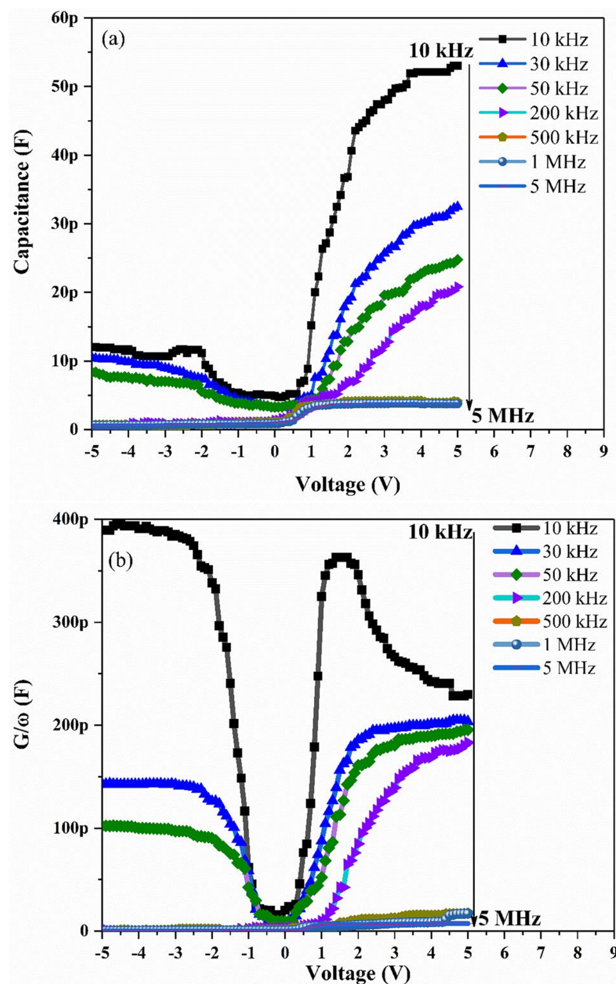

Figure 1. Plots of the (**a**) C–V and (**b**) G/ω–V for the Ag/TiO_2-NW/Ge-NW/Si (MOS) device.

(G/ω) at room-temperature are analyzed. The aim of the work is to investigate to the effect of interface state density (D_{it}), series resistance (R_s) on the C–V and G/ω–V characteristics as well as the dielectric parameters of the proposed MOS device with the applied bias voltage and frequency.

Results and discussion

The C–V and G/ω–V measurements of Ag/TiO_2-NW/Ge-NW/Si MOS device are obtained for different frequencies and voltage ranges at room-temperature as shown in Fig. 1a,b. It is observed from Fig. 1a, that the MOS device displayed extensive distribution in depletion, inversion and accumulation regions. As seen in the figure, the MOS device showed an inversion region (-5 V to 0 V), a depletion region (0 V to 2 V) and an accumulation region (2 V to 5 V) at almost each frequency respectively. The voltage shift is due to the presence of surface states in the MOS device[23]. The measured capacitance (C) and conductance (G/ω) values showed strong dependence on frequency and voltage in the depletion region which might be due to the D_{it} and R_s in the MOS device. The decrease in C and G/ω with the increase in frequency as shown in Fig. 2a,b, might be because the D_{it} cannot follow the alternating current (ac) signal at high frequencies and hence the contribution of these states to capacitance and conductance decrease with the increase in frequency[24]. This makes the contribution of interface state capacitance to the total capacitance negligible[25]. Thus, the measured C–V and G/ω–V values are close to the ideal case at high frequencies. At low frequency, the wide dispersion present in depletion region for both the C–V and G/ω–V curves is due to the existence of D_{it}[26].

The electrical parameters D_{it} and R_s could have attributed to the deviation in both the C–V and G/ω–V curves from the ideal behaviour. The unsymmetrical growth of nanowires due to the shadowing effect inherent in the GLAD technique may have induced inhomogeneous contact during the metallization process between the metal contact and the semiconductor junction. This also could be the reason for the deviation from the ideal behaviour of the MOS device. The Nicollian and Brews method[25] is used to determine the parameters R_s in the measured voltage range of the MOS device. This method is reported to be more precise in comparison with Norde and Cheung functions and conductance and admittance methods as per previous report[26]. R_s is calculated using the Eq. (1) [25] given below:

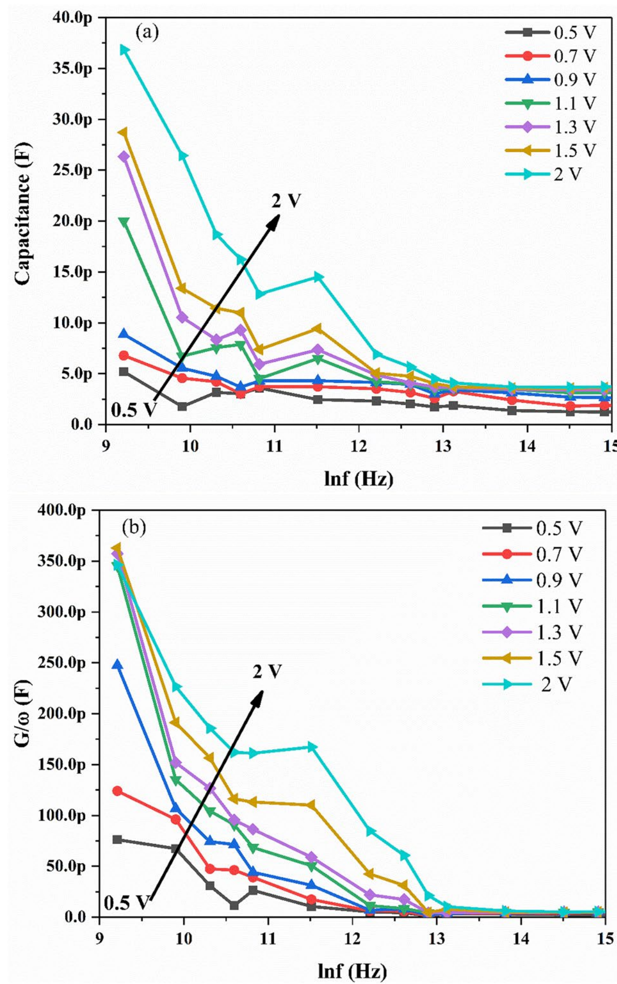

Figure 2. Plots of the (**a**) C-lnf and (**b**) G/ω-lnf for the Ag/TiO_2-NW/Ge-NW/Si (MOS) device.

$$R_s = \frac{G_{ma}}{G_{ma}^2 + (\omega C_{ma})^2} \tag{1}$$

where C_{ma} and G_{ma} are the measured C and G for any biased voltage and ω is the angular frequency. Figure 3a,b, show the R_s–V plots determined from Eq. 1. It is observed from Fig. 3a that R_s decreases with an increase in frequency and the presence of peak around – 0.5 V to 1.3 V at low frequencies is due to the presence of D_{it}. The changes in R_s from region to region clearly shows that R_s is dependent on both the applied frequency and voltage. The change in R_s is evident especially in the inversion and depletion regions from the low to the high frequency range. It should be noted that R_s is independent of frequency at the accumulation region from frequency greater than 30 kHz. Furthermore, the voltage dependent R_s show almost constant value at higher frequencies (frequency > 200 kHz). This shows that for Ag/TiO_2-NW/Ge-NW/Si (MOS) device, the R_s is effective in the accumulation region in high voltage at high frequencies (frequency > 200 kHz).

The D_{it} is another parameter which affects the measured C–V and G/ω–V for the Ag/TiO_2-NW/Ge-NW/Si (MOS) device. The frequency dependent D_{it} plot can be obtained using the Hill-Coleman method from Eq. (2)[27] given below:

$$D_{it} = \frac{2}{qA} \frac{\left(\frac{G_m}{\omega}\right)_{max}}{\left(\frac{\left(\frac{G_m}{\omega}\right)_{max}}{C_{ox}}\right)^2 + \left(1 - \frac{C_m}{C_{ox}}\right)^2} \tag{2}$$

where C_{ox} and $(G_m/\omega)_{max}$ are the interlayer capacitance, maximum value of conductance which is corresponding to C_m and the value of C_{ox} can be calculated from the measured C and G/ω values at the strong accumulation region using Eq. (3)[28] as given below:

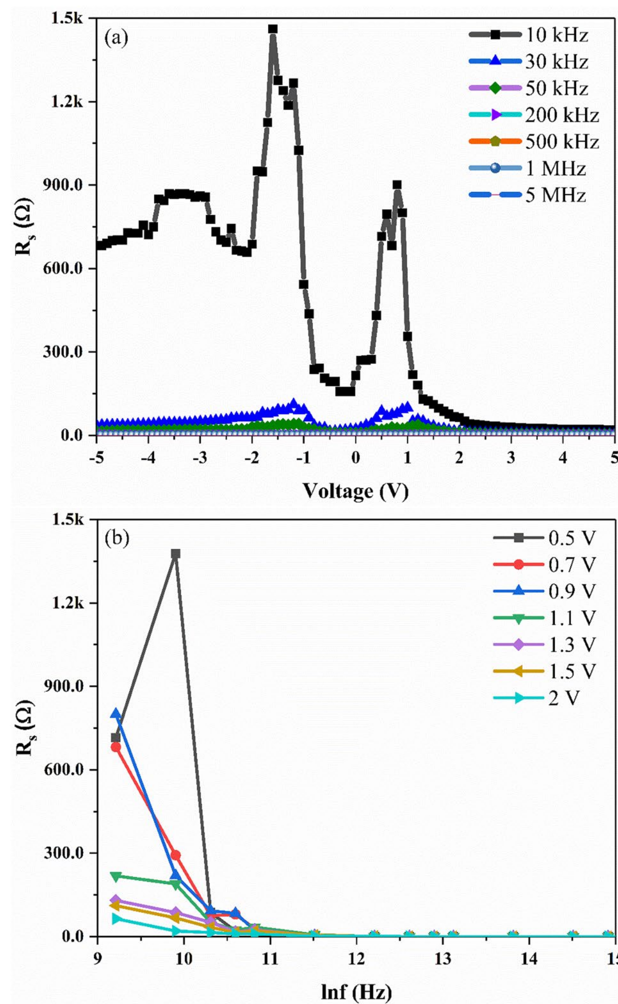

Figure 3. Plots of (**a**) R_s–V and (**b**) R_s-lnf for the Ag/TiO_2-NW/Ge-NW/Si (MOS) device.

$$C_{ox} = C_{ma}\left(1 + \left(\frac{G_{ma}}{\omega C_{ma}}\right)^2\right) \tag{3}$$

The frequency dependent D_{it} determined using Eqs. 2 and 3 is shown in Fig. 4. It is observed that the D_{it} decreases with an increase in frequency for the Ag/TiO_2-NW/Ge-NW/Si (MOS) device which is due to the low power follow rate at high frequencies[28]. Furthermore, the obtained D_{it} value at high frequency (frequency > 400 kHz) is found to be better in comparison with the reported values[17,29,30] and thus addresses the serious issue of high interface state densities. The distinct peak seen in the D_{it} plot in Fig. 4 (inset) at 100 kHz and 300 kHz having D_{it} values of 1.73×10^{13} eV^{-1} cm^{-2} and 2.05×10^{10} eV^{-1} cm^{-2} with defect lifetime of ~ 10 µs and 3.3 µs, respectively. The difference in the lifetime of the defects observed from the D_{it} plot is primarily due to the slow traps and fast traps also known as interface traps corresponding to large defect lifetime and small defect lifetime, respectively[29]. It can be seen that the maximum value of C_m decreases with an increase in R_s which is in good agreement with the theoretical results stated by Chattopadhyay et al.[31]. Therefore, D_{it} at low frequency in the Ag/TiO_2-NW/Ge-NW/Si (MOS) device can follow the ac signal and yield an excess capacitance, thus resulting in D_{it} being more pronounced compared to R_s. In contrast to the low frequency values, the D_{it} values at high frequency cannot follow the ac signal which makes the contribution of interface state capacitance to total capacitance negligible. This results in the contribution of R_s being more pronounced.

In order to obtain the corrected capacitance (C_c) and corrected conductance (G_c/ω) at different frequencies both measured C and G/ω are corrected considering the effect of series resistance (R_s) using the Eq. (4–6)[28] given below:

$$C_c = \frac{\left[G_m^2 + (\omega C_m)^2\right] C_m}{a^2 + (\omega C_m)^2} \tag{4}$$

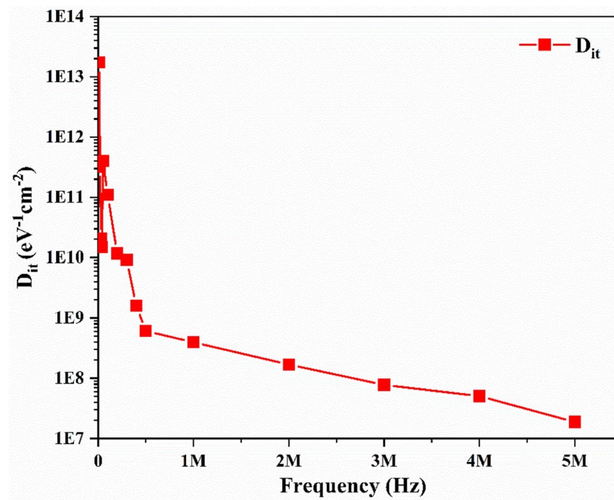

Figure 4. Frequency dependent D_{it} plot for the Ag/TiO_2-NW/Ge-NW/Si (MOS) device.

$$G_c = \frac{G_m^2 + (\omega C_m)^2 a}{a^2 + (\omega C_m)^2} \tag{5}$$

$$a = G_m - \left[G_m^2 + (\omega C_m)^2\right] R_s \tag{6}$$

Figure 5 represents the C_{C-V} and G_c/ω–V plots for the Ag/TiO_2-NW/Ge-NW/Si (MOS) device. It is observed after making the correction that is considering the effect of R_s in C_c versus V plot, there is no significant change in the corrected capacitance (C_c) values. However in the case of the corrected conductance (G_c), it is observed that there is a decrease in the C_c value with an increase in frequency and the existence of peaks in the G_c/ω–V plot confirms the charge transfer taking place at the interface[28].

The dependence of the dielectric constant (ϵ'), dielectric loss (ϵ'') and dielectric loss tangent (tan(δ)) on the frequency and voltage are investigated in various frequencies (10 kHz to 5 MHz) at different voltage ranges (-5 V to 5 V) at room-temperature. The values of the dielectric constant (ϵ') and dielectric loss (ϵ'') of the Ag/TiO_2-NW/Ge-NW/Si (MOS) device are obtained using the measured C, G/ω, thickness of the oxide layer, area of diode and permittivity of free space (ϵ_o). The complex dielectric constant ($\varepsilon * = \varepsilon' - j\varepsilon''$), the real and imaginary parts could then be determined from the relations given in Eq. (7–8)[32] given below:

$$\varepsilon' = \frac{C_{ox}}{C_o} \tag{7}$$

$$\varepsilon'' = \frac{d_{ox}}{A\varepsilon_o}\frac{G_m}{\omega} = \frac{G_m}{C_o\omega} \tag{8}$$

where $C_o = \varepsilon_o\left(\frac{A}{d_{ox}}\right)$; A is the area of the device, d_{ox} is the oxide layer thickness, ϵ_o is the permittivity of free space ($\epsilon_o = 8.85 \times 10^{-14}$ F/cm), G_m is the conductivity of MOS structure and ω is the angular frequency and j is the imaginary root of – 1. The dielectric loss tangent can be determined by the relation given in Eq. (9)[32] given below:

$$\tan\delta = \frac{\varepsilon''}{\varepsilon'} \tag{9}$$

Both the real and imaginary parts are calculated from the measured C and G/ω. The dielectric loss is expressed as the energy loss caused by the heating of a dielectric material in a variable electric field[26]. The loss factor is known as the energy spent at the dielectric to avoid bound charge displacement to be in phase with the field alternations[26]. From Fig. 6a-c, it is observed that the ϵ', ϵ'' and tan(δ) values show independent behaviour from frequency in the inversion region and then starts to increase from the depletion region to the accumulation region. Furthermore, the ϵ', ϵ'' and tan(δ) values decrease with increasing frequency. This behaviour can be explained by the fact that when the frequency is increased, the interfacial dipoles in the dielectric have less time to orient themselves in the direction of the alternating electric field and alternatively, the polarization decreases with the increase in frequency and remains constant[26]. This implies that at higher frequencies, the contribution of D_{it} and dipole polarization could be neglected. In other words, the decrement in the ϵ' is due to the fact that the dipoles do not have enough time to orient themselves in the direction of electric field and the D_{it} cannot follow the ac signal. Furthermore, the mix-phase established from the XRD plot, where both anatase and rutile type TiO_2 are reported might also be the reason behind the decrement in the ϵ'[33]. The broad peak observed in the tan(δ) plot at frequencies less than 200 kHz could be attributed to the relaxation process and the D_{it}. In addition,

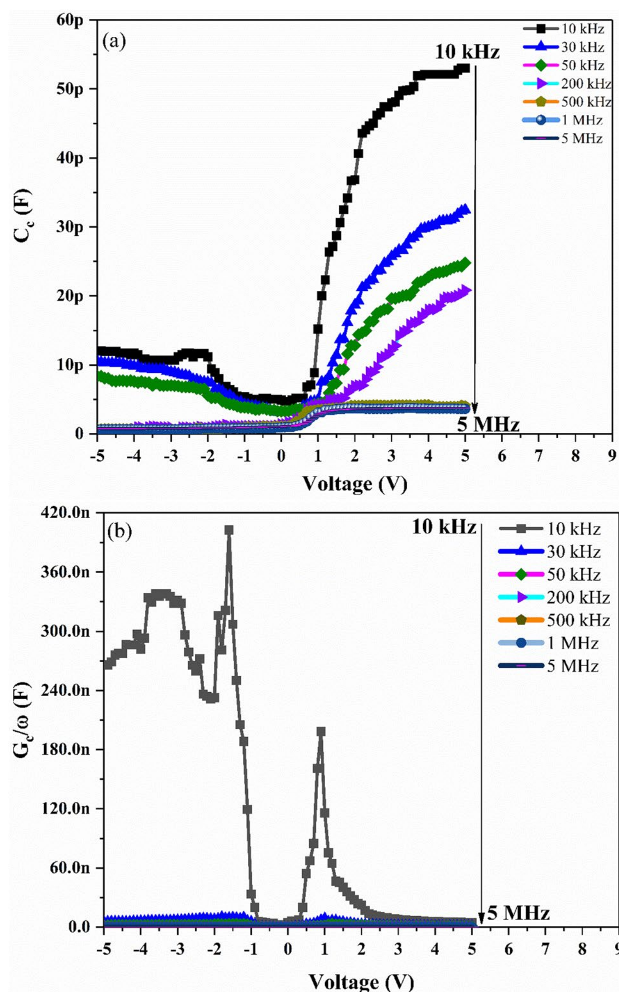

Figure 5. Plots of the (**a**) $C_{C\text{-}V}$ and (**b**) G_c/ω–V for the Ag/TiO_2-NW/Ge-NW/Si (MOS) device.

the behaviour of decrease in the values of the measured capacitance (C), dielectric constant (ϵ') and dielectric loss (ϵ'') decreases with the increase in frequency is attributed to the presence of the interfacial polarization mechanism[28]. Moreover, to show the effect of voltage on the dielectric parameters, frequency dependent plots are shown in Fig. 7a-c at different bias voltage, respectively. It is observed that the decrease in values of ϵ', ϵ'' and tan(δ) with the increase in frequency is due to the decrease in polarization with the increase in frequency and the values remains constant at high frequency. This implies that the contribution of dipole polarization and D_{it} could be neglected at high frequency. Therefore, the D_{it} cannot follow the ac signal and the absence of any interfacial polarization mechanism in the MOS device makes the contribution to C, ϵ' and ϵ'' negligible at high frequencies (> 200 kHz). The low frequency dielectric behaviour of the MOS device can be attributed to four possible mechanisms: electrode interface, dc conductivity, dipole-orientation and charge carriers[34].

Experimental procedure

TiO_2-NW/Ge-NW is fabricated on a 1 cm × 1 cm n-type Si (100) substrate using the GLAD technique incorporated into an electron-beam evaporator (Vacuum Coating Unit Model-BC-300). Using an ultra-sonicator, the Si substrates are cleaned in a 3-step sequence using electronic grade acetone, methanol, and rinsed with de-ionized (DI) water. During the synthesis process, the base pressure of ~ 2×10^{-6} mbar is maintained inside the electron-beam chamber. A deposition rate of 0.5 Å s^{-1} is maintained during the synthesis of TiO_2-NW/Ge-NW using a digital thickness monitor (DTM). Firstly, a thin-film (TF) layer of Ge (30 nm) is deposited over the Si substrate using a pure 99.999% Ge source. Next the substrate is azimuthally rotated at.

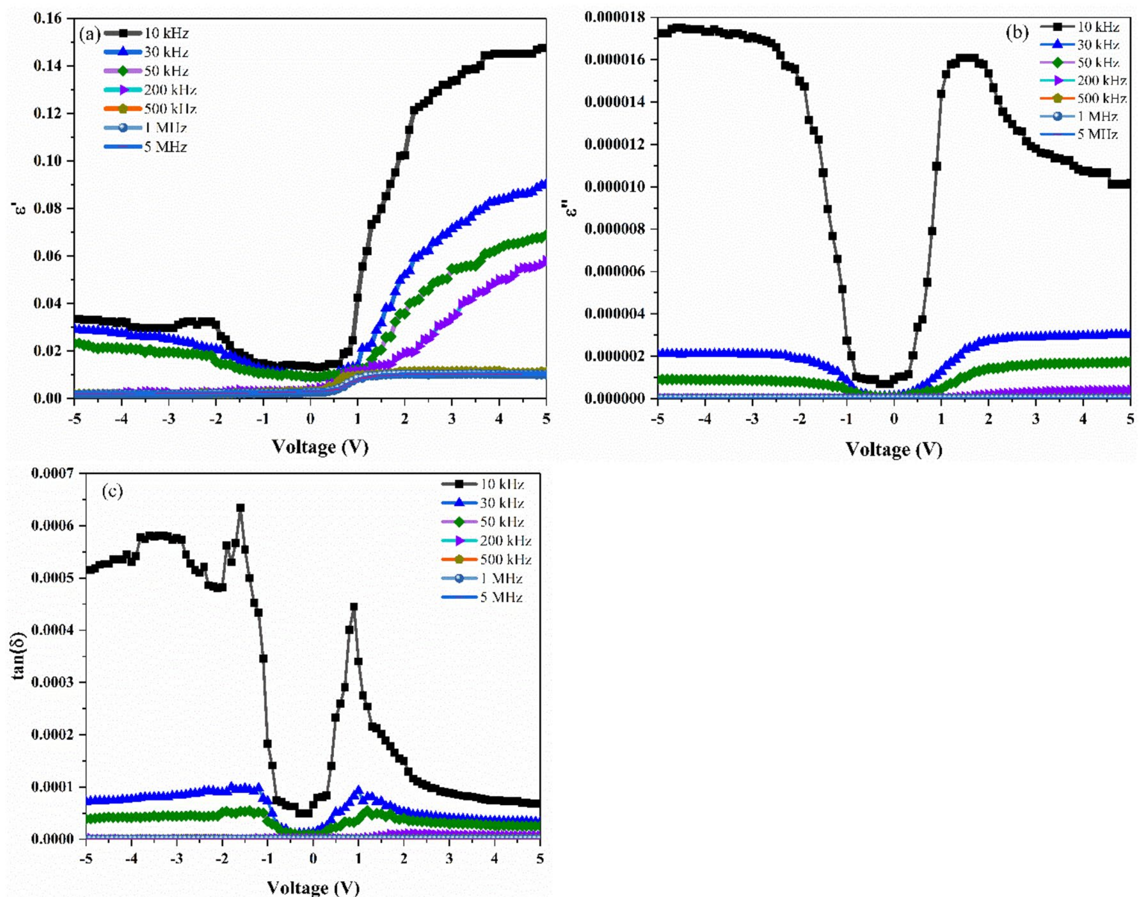

Figure 6. Plot of (**a**) ϵ′–V, (**b**) ϵ″–V, (**c**) tan(δ)–V for the Ag/TiO_2-NW/Ge-NW/Si (MOS) device.

30 rpm with substrate holder kept inclined at 85° with respect to the source where Ge-NW (200 nm) was synthesized. Subsequently the TiO_2-NW (200 nm) is fabricated using pure 99.999% TiO_2 source over the Ge-NW to obtain coaxial TiO_2-NW/Ge-NW assembly. Finally, silver (Ag) metal contacts are fabricated using an aluminum mask with a hole area ~ 7 mm^2 on both the samples. The schematic of the Ag/TiO_2-NW/Ge-NW/Si MOS device is given in Fig. 8a-d. The electrical characterization of the devices is performed using a Keithly 4200 SCS from 10 kHz to 5 MHz.

Conclusion

The electrical and dielectric parameters of a GLAD synthesized Ag/TiO_2-NW/Ge-NW/Si (MOS) device have been studied over a wide frequency and voltage ranges. It has been determined from the measured C and G/ω behaviour of the MOS device that the parameters were dependent on the applied frequencies and voltages. In addition, the wide dispersion exhibited in both C and G/ω curves in the depletion region was mainly attributed to the existence of the D_{it}. Furthermore, the measured C and G/ω behaviour with the applied frequency and voltage were dependent on the D_{it}, R_s and the polarization process. The D_{it} and R_s parameters were computed using the Hill-Coleman and Nicollian–Brews methods in wide frequency and voltage ranges. The dielectric properties analysis of the MOS device established that the ϵ′, ϵ″ and tan(δ) parameters were dependent on frequency and that the values decrease with the increase in frequency. Furthermore, it is observed at higher frequencies (> 200 kHz), the ϵ′ and ϵ″ values remains constant which is attributed to the interfacial polarization. Moreover, the decrement in the ϵ′ value for the MOS device is also due to the mix-phase of anatase and rutile type TiO_2 present in the structure as determined from the XRD study reported earlier. Therefore, the study of the proposed MOS device has highlighted that it offers improved device capability for opto-electronics applications and also the potential for further improvement to obtain better device performance.

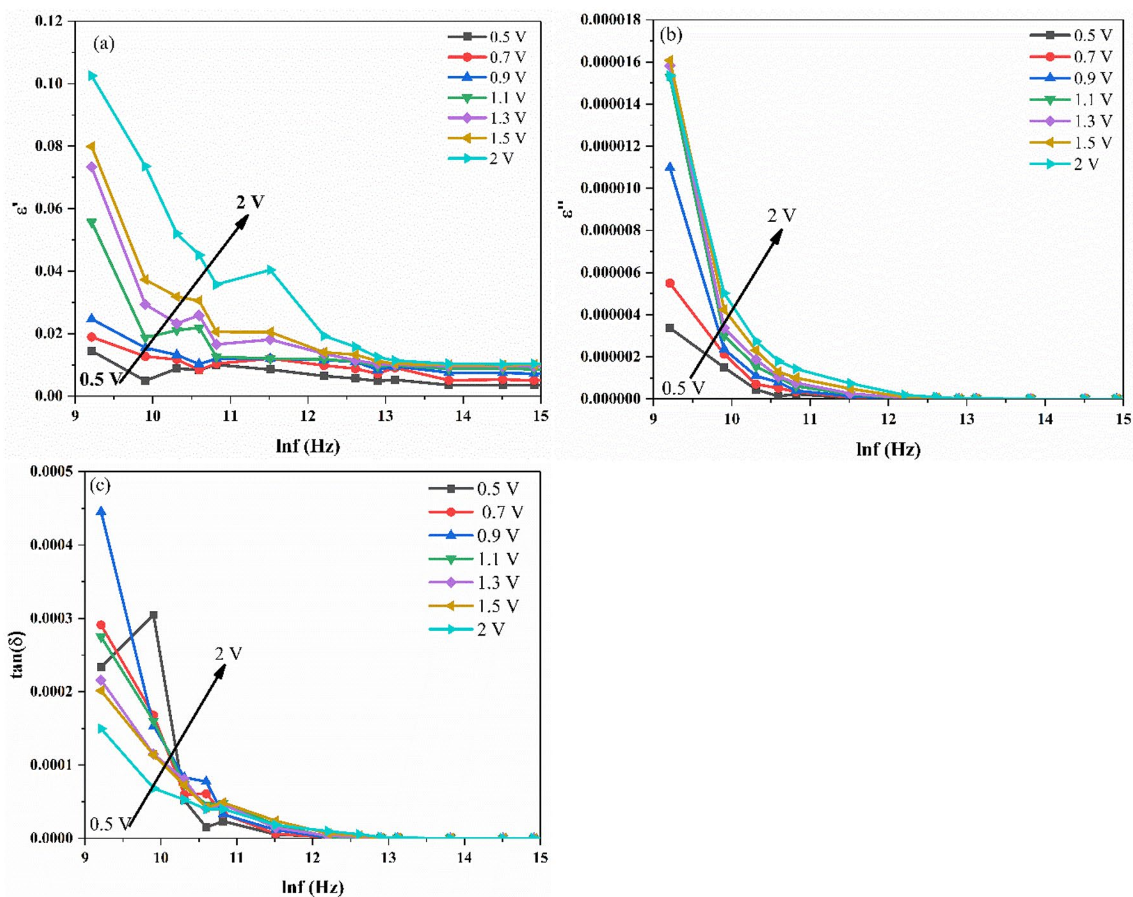

Figure 7. Plot of (**a**) ϵ′ versus lnf, (**b**) ϵ″ versus lnf, (**c**) tan(δ) versus lnf for the Ag/TiO_2-NW/Ge-NW/Si (MOS) device.

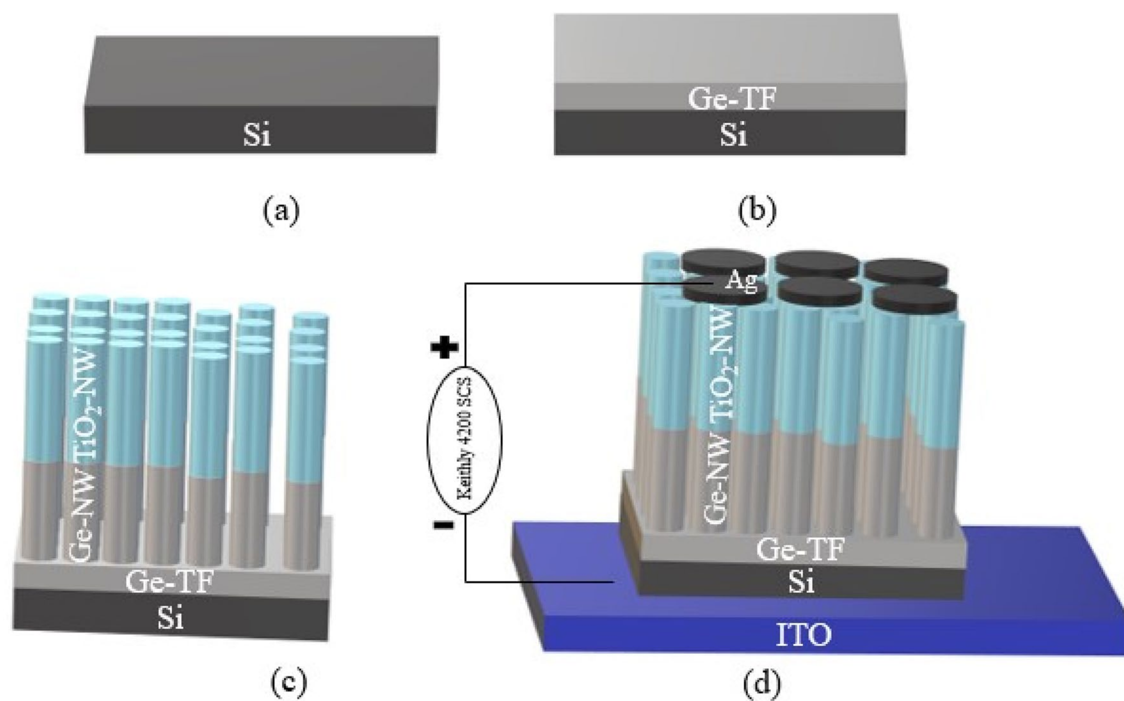

Figure 8. (**a**) Si wafer, (**b**) Synthesis of Ge-TF, (**c**) Synthesis of TiO_2-NW/Ge-NW/Si using GLAD technique, (**d**) Synthesis of Ag/TiO_2-NW/Ge-NW/Si (MOS) device schematic.

Data availability

The datasets generated during and/or analysed during the current study are available from the corresponding author on reasonable request.

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References

1. Kim, C. *et al.* Highly responsive near-infrared photodetector with low dark current using graphene/germanium Schottky junction with Al_2O_3 interfacial layer. *Nanophotonics* **10**, 1573–1579 (2021).
2. Pooja, P. & Chinnamuthu, P. Annealed n-TiO_2/In_2O_3 nanowire metal-insulator-semiconductor for highly photosensitive low-noise ultraviolet photodetector. *J. Alloys Compd.* **854**, 157229 (2021).
3. Chandra, A. *et al.* NIR photodetector based on p-silicon nanowires/n-cadmium sulfide nanoscale junctions. *Appl. Surf. Sci.* **548**, 149256 (2021).
4. Shougaijam, B., Ngangbam, C. & Lenka, T. R. Enhancement of broad light detection based on annealed Al-NPs assisted TiO_2-NWs deposited on p-Si by GLAD technique. *IEEE Trans. Nanotechnol.* **17**, 285–292 (2018).
5. Chinnamuthu, P., Dhar, J. C., Mondal, A., Bhattacharyya, A. & Singh, N. K. Ultraviolet detection using TiO_2 nanowire array with Ag Schottky contact. *J. Phys. D. Appl. Phys.* **45**, 135102 (2012).
6. Liu, K., Sakurai, M., Liao, M. & Aono, M. Giant improvement of the performance of ZnO nanowire photodetectors by Au nanoparticles. *J. Phys. Chem. C* **114**, 19835–19839 (2010).
7. Yang, W. *et al.* Silicon-compatible photodetectors: Trends to monolithically integrate photosensors with chip technology. *Adv. Funct. Mater.* **29**, 1808182 (2019).
8. Singh, N. K. *et al.* 2D like photonic crystal using In_2O_3–SiO_x heterostructure nanocolumn arrays and humidity sensing. *Electron. Mater. Lett.* **10**, 975–980 (2014).
9. Mahala, P. *et al.* High-performing self-driven ultraviolet photodetector by TiO_2/Co_3O_4 photovoltaics. *J. Alloys Compd.* **827**, 154376 (2020).
10. Lahiri, R. & Mondal, A. Superior memory of Er-doped TiO_2 nanowire MOS capacitor. *IEEE Electron Device Lett.* **39**, 1856–1859 (2018).
11. Panigrahy, S. & Dhar, J. C. Non-volatile memory property of Er_2O_3 doped SnO_2 nanowires synthesized using GLAD technique. *J. Mater. Sci. Mater. Electron.* **30**, 8339–8347 (2019).
12. Dimoulas, A. *et al.* Interface engineering for Ge metal-oxide-semiconductor devices. *Thin Solid Films* **515**, 6337–6343 (2007).
13. Moreau, M. *et al.* Investigation of capacitance–voltage characteristics in Ge/high-κ MOS devices. *J. Non. Cryst. Solids* **355**, 1171–1175 (2009).
14. Kamata, Y. High-k/Ge MOSFETs for future nanoelectronics. *Mater. Today* **11**, 30–38 (2008).
15. Bengi, A., Aydemir, U., Altindal, Ş, Özen, Y. & Özçelik, S. A comparative study on the electrical characteristics of Au/n-Si structures with anatase and rutile phase TiO_2 interfacial insulator layer. *J. Alloys Compd.* **505**, 628–633 (2010).
16. Kim, G. S. *et al.* Effective Schottky barrier height lowering of metal/n-Ge with a TiO_2/GeO_2 interlayer stack. *ACS Appl. Mater. Interfaces* **8**, 35419–35425 (2016).
17. Khan, Z. N., Khan, S. A. & Shakeel, S. Incorporation of Ge on high K dielectric material for different fabrication technologies (HBT, CMOS) and their impact on electrical characteristics of the device. *J. Nanomater.* **2018**, (2018).
18. Rahman, M. S. & Evangelou, E. K. Dielectric relaxation and charge trapping characteristics study in Germanium based MOS devices with HfO_2/Dy_2O_3 gate stacks. *IEEE Trans. Electron Devices* **58**, 3549–3558 (2011).
19. Singh, H. M., Choudhuri, B. & Chinnamuthu, P. Investigation of optoelectronic properties in germanium nanowire integrated silicon substrate using kelvin probe force microscopy. *IEEE Trans. Nanotechnol.* **19**, 1–1 (2020).
20. Panigrahy, S. & Dhar, J. C. Suppression of leakage current using annealed Er_2O_3 nanowires as a superior dielectric material. *J. Mater. Sci. Mater. Electron.* **32**, 3522–3528 (2021).
21. Rajkumari, R. & Singh, N. K. Ag nanoparticle-decorated WO_3 nanowires for nonvolatile memory. *ACS Appl. Nano Mater.* **3**, 12087–12094 (2020).
22. Zhao, Y., Ye, D., Wang, G.-C. & Lu, T.-M. Designing nanostructures by glancing angle deposition. In *Nanotubes and Nanowires* vol. 5219 59–73 (International Society for Optics and Photonics, 2003).
23. Tataroğlu, A. & Altindal, Ş. Characterization of current-voltage (I–V) and capacitance–voltage–frequency (C–V–f) features of Al/SiO_2/p-Si (MIS) Schottky diodes. *Microelectron. Eng.* **83**, 582–588 (2006).
24. Tanrıkulu, E. E., Demirezen, S., Altındal & Uslu, I. On the anomalous peak and negative capacitance in the capacitance–voltage (C–V) plots of Al/(%7 Zn-PVA)/p-Si (MPS) structure. *J. Mater. Sci. Mater. Electron.* **29**, 2890–2898 (2018)
25. Nicollian, E. H. & Goetzberger, A. MOS conductance technique for measuring surface state parameters. *Appl. Phys. Lett.* **7**, 216–219 (1965).
26. Demirezen, S., Eroğlu, A., Azizian-Kalandaragh, Y. & Altındal, Ş. Electric and dielectric parameters in Au/n-Si (MS) capacitors with metal oxide-polymer interlayer as function of frequency and voltage. *J. Mater. Sci. Mater. Electron.* **31**, 15589–15598 (2020).
27. Hill, W. A. & Coleman, C. C. A single-frequency approximation for interface-state density determination. *Solid State Electron.* **23**, 987–993 (1980).
28. Yücedağ, I., Altindal, Ş & Tataroğlu, A. On the profile of frequency dependent series resistance and dielectric constant in MIS structure. *Microelectron. Eng.* **84**, 180–186 (2007).
29. Kuzum, D. *et al.* High-mobility Ge N-MOSFETs and mobility degradation mechanisms. *IEEE Trans. Electron Devices* **58**, 59–66 (2011).
30. Zhang, L. *et al.* Selective passivation of GeO_2/Ge interface defects in atomic layer deposited high-k MOS structures. *ACS Appl. Mater. Interfaces* **7**, 20499–20506 (2015).
31. Chattopadhyay, P. & RayChaudhuri, B. Frequency dependence of forward capacitance-voltage characteristics of Schottky barrier diodes. *Solid State Electron.* **36**, 605–610 (1993).
32. Demirezen, S. Frequency- and voltage-dependent dielectric properties and electrical conductivity of Au/PVA (Bi-doped)/n-Si Schottky barrier diodes at room temperature. *Appl. Phys. A Mater. Sci. Process.* **112**, 827–833 (2013).
33. Manas, S. H., Choudhuri, B. & Chinnamuthu, P. Reduction of interface state density in coaxial TiO_2/Ge nanowire assembly-based heterostructure and superior photodetection. *J. Alloys Compd.* **853**, 157344 (2021).
34. Fanggao, C. *et al.* Temperature and frequency dependencies of the complex dielectric constant of poly(ethylene oxide) under hydrostatic pressure. *J. Polym. Sci. Part B Polym. Phys.* **34**, 425–433 (1996).

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Author contributions

H.M.S performed the investigation, data curation, formal analysis and written the original draft. L.Y.Y contributed in review and editing of the original draft. P.C, the corresponding author conceptualize, provided supervision, validation, review and editing of the original draft. All authors reviewed the manuscript.

Competing interests

The authors declare no competing interests.

Additional information

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