

SCIENTIFIC REPORTS

OPEN

Effects of H₂ High-pressure Annealing on HfO₂/Al₂O₃/In_{0.53}Ga_{0.47}As Capacitors: Chemical Composition and Electrical Characteristics

Sungho Choi¹, Youngseo An¹, Changmin Lee¹, Jeongkeun Song¹, Manh-Cuong Nguyen², Young-Chul Byun³, Rino Choi², Paul C. McIntyre⁴ & Hyongsu Kim^{1,5}

We studied the impact of H₂ pressure during post-metallization annealing on the chemical composition of a HfO₂/Al₂O₃ gate stack on a HCl wet-cleaned In_{0.53}Ga_{0.47}As substrate by comparing the forming gas annealing (at atmospheric pressure with a H₂ partial pressure of 0.04 bar) and H₂ high-pressure annealing (H₂-HPA at 30 bar) methods. In addition, the effectiveness of H₂-HPA on the passivation of the interface states was compared for both p- and n-type In_{0.53}Ga_{0.47}As substrates. The decomposition of the interface oxide and the subsequent out-diffusion of In and Ga atoms toward the high-*k* film became more significant with increasing H₂ pressure. Moreover, the increase in the H₂ pressure significantly improved the capacitance–voltage characteristics, and its effect was more pronounced on the p-type In_{0.53}Ga_{0.47}As substrate. However, the H₂-HPA induced an increase in the leakage current, probably because of the out-diffusion and incorporation of In/Ga atoms within the high-*k* stack.

For high-speed metal-oxide-semiconductor field-effect transistors (MOSFETs) with a technology node of less than 5 nm, In_{1-x}Ga_xAs has been considered the most promising channel layer as a replacement for conventional Si because of its various merits such as high electron mobility, large band gap, and small lattice mismatch with InP (for practical device integration on a Si wafer)^{1–3}. Therefore, tremendous efforts have been made to engineer the atomic layer deposition (ALD) of high-*k* dielectrics on In_{1-x}Ga_xAs and to improve the electrical properties of MOS capacitors using various pre- and/or post-deposition processes.

Since the use of conventional Si-channel MOSFET devices, post-metallization annealing (PMA), also termed as forming gas annealing (FGA) and typically performed at 300–400 °C in a N₂ atmosphere mixed with a small amount of H₂, has been the most effective method for passivating the interface states (specifically, the dangling bonds) located within a Si band gap^{4–6}. Similarly, a decrease in the interface state density (*D*_{it}) has been achieved for MOS capacitors made of high-*k* dielectrics deposited on III-V channel materials, including In_{1-x}Ga_xAs, by FGA^{7–9}. In addition, a further reduction in *D*_{it} could be achieved for high-*k*/n-type In_{1-x}Ga_xAs MOS capacitors using H₂ high-pressure annealing (H₂-HPA)¹⁰, whose effectiveness has been demonstrated in a high-*k*/Si system^{11–13}. However, its effectiveness on In_{1-x}Ga_xAs substrates with different doping types was not compared in detail.

Many studies have experimentally evidenced the adverse effects of PMA such as substantial out-diffusion of components from the III-V interface oxide toward the high-*k* film in various high-*k*/III-V MOS capacitors^{14–20}. For instance, Krylov *et al.*^{14,15} observed leakage current degradation of Al₂O₃ on In_{0.53}Ga_{0.47}As after N₂ annealing/FGA at 400 °C and attributed it to significant In out-diffusion. The out-diffusion of Ga and As was also noted at

¹School of Advanced Materials Science and Engineering, Sungkyunkwan University, Suwon, 16419, Republic of Korea. ²Department of Materials Science and Engineering, Inha University, Incheon, 22212, Republic of Korea. ³ASM International, Phoenix, AZ, 85034, USA. ⁴Department of Materials Science and Engineering, Stanford University, Stanford, CA, 94305, USA. ⁵SKKU Advanced Institute of Nanotechnology (SAINT), Sungkyunkwan University, Suwon, 16419, Republic of Korea. Correspondence and requests for materials should be addressed to H.K. (email: hsubkim@skku.edu)

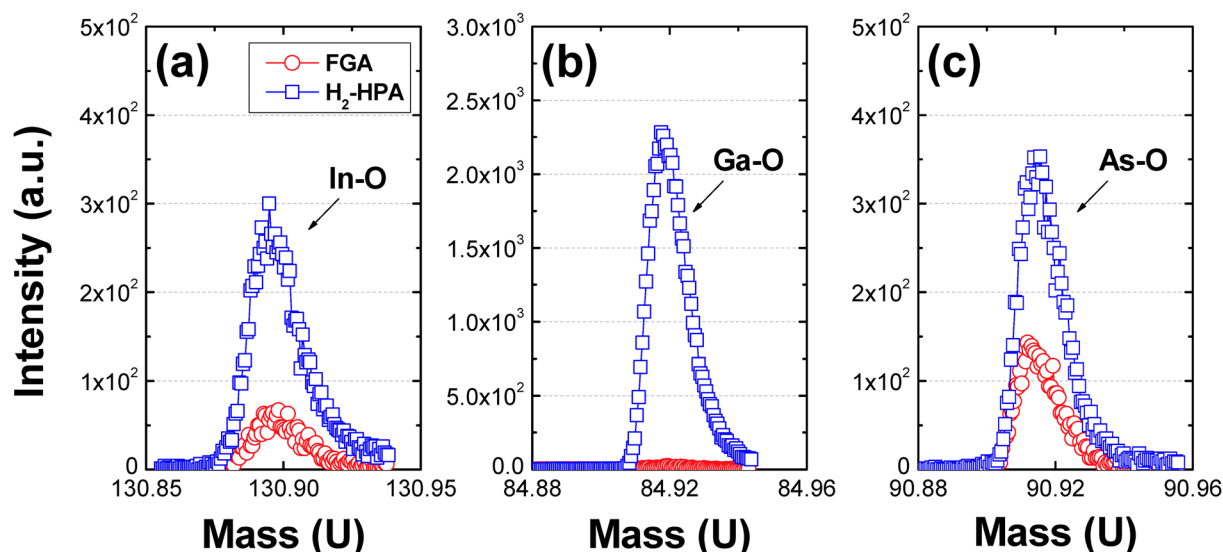


Figure 1. Changes in the ToF-SIMS intensities of (a) In, (b) Ga, and (c) As collected from the surface of the $\text{HfO}_2/\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ samples with different PMA conditions.

higher temperatures of 400–700 °C under N_2 atmosphere¹⁶. For HfO_2 dielectrics on $\text{In}_{1-x}\text{Ga}_x\text{As}$, both In and Ga out-diffusion occurred at temperatures higher than 400 °C¹⁷, and In desorption/migration was enhanced by FGA at temperatures as low as 350 °C¹⁸.

Herein, we studied the effect of H_2 pressure on the chemical/electrical properties of $\text{HfO}_2/\text{Al}_2\text{O}_3$ gate dielectrics deposited *via* ALD on HCl wet-cleaned $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrates. Possible out-diffusion of the substrate elements and their subsequent incorporation into the high- k film were examined with different H_2 pressures using conventional FGA (at atmospheric pressure using 4% H_2 in N_2) and H_2 -HPA (at 30 bar using 100% H_2) methods. Furthermore, for a detailed study of their respective effects on the electrical characteristics of MOS capacitors, both p- and n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrates were used.

Results and Discussion

Chemical Composition. First, the compositional changes in the $\text{HfO}_2/\text{Al}_2\text{O}_3$ gate dielectric due to different PMA conditions (FGA at atmospheric pressure using 4% H_2 gas balanced with N_2 and H_2 -HPA at 30 bar using 100% H_2 gas) were examined using time-of-flight secondary ion mass spectrometry (ToF-SIMS) and angle-resolved X-ray photoelectron spectroscopy (ARXPS), and the results are shown in Figs 1 and 2, respectively. A thin dielectric stack of 2 nm $\text{HfO}_2/1$ nm Al_2O_3 was intentionally used because of the short information depth of XPS measurements, whereas ToF-SIMS was used to detect the chemical change on the high- k surface to a depth of couple of angstroms. Although the thinness of the gate dielectric stack and the PMA performed in the absence of a gate metal electrode might yield results different from those of the thicker dielectrics used for electrical characterization, it is believed that a relative comparison would be possible between the samples with different PMA conditions. According to the ToF-SIMS data shown in Fig. 1, some amounts of substrate elements, mainly In and As, were detected on the sample surface after FGA, which indicated that the out-diffusion of the substrate elements occurred during the ALD²¹ and/or the subsequent FGA process^{9, 14, 18, 19, 22}. When the H_2 pressure was increased to 30 bar, the concentrations of In, Ga, and As atoms on the high- k surface increased significantly as compared to those in the FGA (H_2 partial pressure of 0.04 bar) sample. This suggests that the H_2 pressure strongly affects the out-diffusion of the substrate elements. This was further confirmed by ARXPS measurements, as shown in Fig. 2; additional comparison with the H_2 -HPA sample annealed at a different H_2 pressure of 10 bar can be found in Figure S1 (Supplementary Information). As the H_2 pressure was increased, both In and Ga atoms (in their oxidized states) significantly diffused toward the dielectric surface; this verified the ToF-SIMS result. In contrast, no significant change was observed in the intensity of the As-O peaks in the depth direction of the As 3d spectrum for different PMA conditions. Because the chemical information of the bulk region above the interface was also gathered at the highest take-off angle of 90°, it was difficult to differentiate the possible change in the amount of interfacial oxide while varying the H_2 pressure.

The $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrate was exposed to air after the removal of native oxide by wet chemical cleaning, and the subsequent ALD high- k process was carried out in a highly oxidizing atmosphere at an elevated temperature. Therefore, it is most likely that an abrupt interface between the high- k and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ was not realized²³, and the formation of In- and Ga-oxides was thermodynamically preferred to that of As-oxide²⁴. As suggested by several researchers^{24–26}, the formed interfacial In- and Ga-oxides can be decomposed by atomic hydrogen at temperatures as low as 400 °C. Therefore, a high H_2 pressure could accelerate their decomposition and the subsequent release of In/Ga-related species into the high- k film. Similar to this result, Cabrera *et al.*¹⁸ observed an enhanced decomposition of the interface oxide and the subsequent out-diffusion of In atoms in a $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ system when the PMA ambient (at atmospheric pressure) was changed from pure N_2 to 5% H_2 at 350 °C. However,

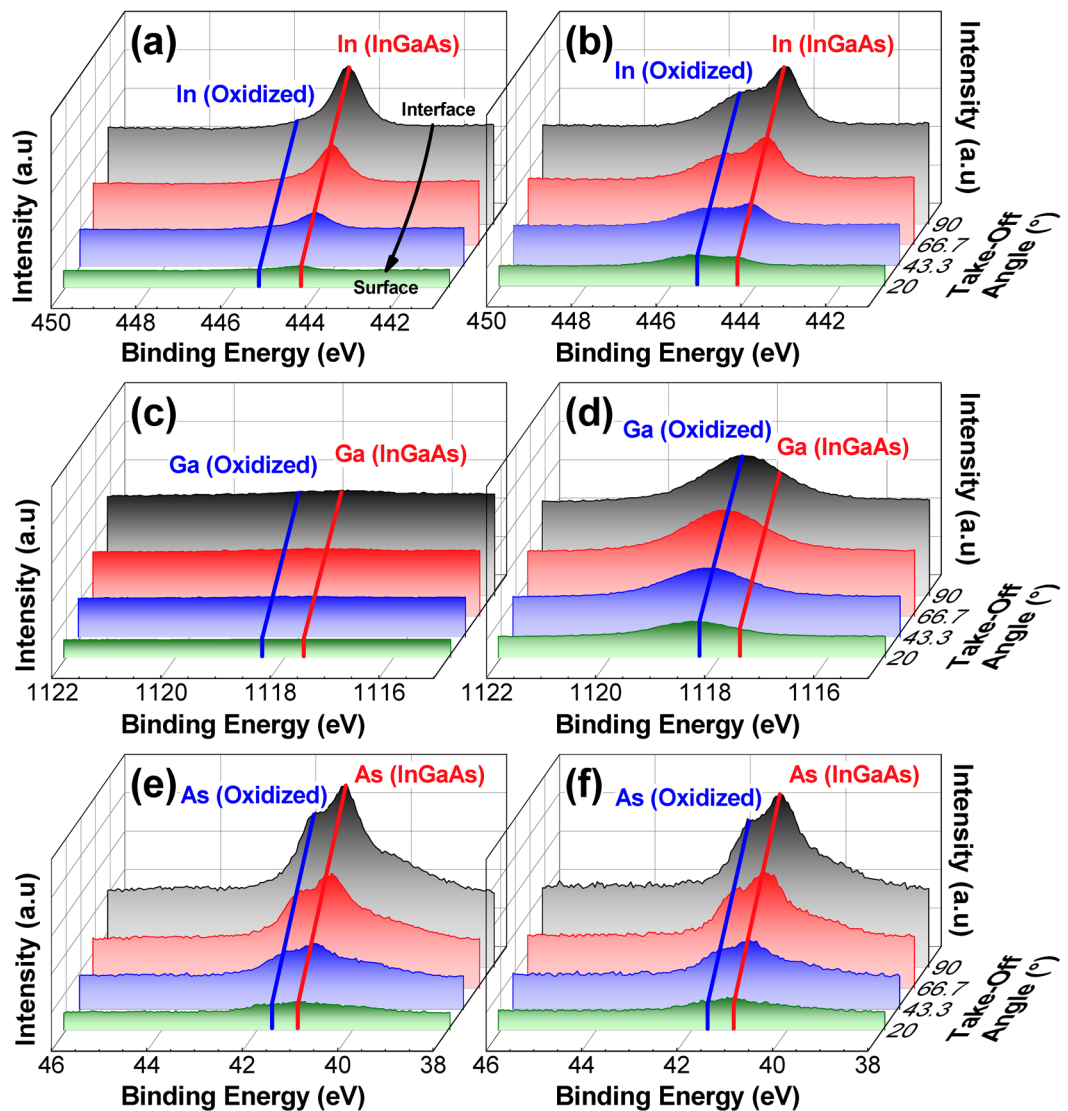


Figure 2. Angle-resolved XPS spectra of (a,b) In 3d, (c,d) Ga 2p, and (e,f) As 3d peaks measured from the $\text{HfO}_2/\text{Al}_2\text{O}_3$ films on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ after PMA at 400 °C for 30 min: (a,c,e) FGA and (b,d,f) H_2 -HPA.

they did not observe noticeable Ga out-diffusion¹⁸. The contradictory result might be because of differences in the FGA temperature, the use of characterization tools with different detection limits, and the H_2 pressure. On the other hand, As atoms preferred to diffuse out fast in a gaseous state at low temperatures with some amount of aggregation at the high- k /III-V interfaces²⁰. Therefore, the increase in the H_2 pressure may not significantly affect its distribution within the bulk region of the high- k gate stack, as observed from the ARXPS measurement (Fig. 2). Instead, a slight enrichment of As atoms on the high- k surface occurred, as observed from the ToF-SIMS measurement (Fig. 1). Because the out-diffused In/Ga-related species might exist in an oxidized form and produce point defects in the high- k film, they may generate additional trap energy levels in the band gap of the high- k film, which might degrade the electrical properties of the high- k film itself, such as the leakage current and reliability, rather than increasing D_{it} .

Electrical Characteristics. For electrical characterization of the $\text{HfO}_2/\text{Al}_2\text{O}_3$ dielectrics on both p- and n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ after PMA at different H_2 pressures, HfO_2 and Al_2O_3 layers with thicknesses of approximately 4.5 and 1.0 nm, respectively, were deposited and MOS capacitors were fabricated. Figure 3 shows the capacitance–voltage (C – V) characteristics of the MOS capacitors fabricated on the p- and n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrates after PMA at different H_2 pressures. In addition to quasi-static (QS) C – V measurements, a series of high-frequency C – V measurements were carried out at frequencies varying from 100 Hz to 1 MHz. The flat band voltage (V_{FB}) was extracted using the inflection point method^{27, 28} and was included in the C – V graphs of the n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ samples shown in Fig. 3. For the p-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ samples, it was difficult to determine the accurate V_{FB} values due to a significantly large frequency dispersion at the flat band condition. In the case of the reference samples (FGA samples), a large frequency-dependent hump from depletion to inversion regions

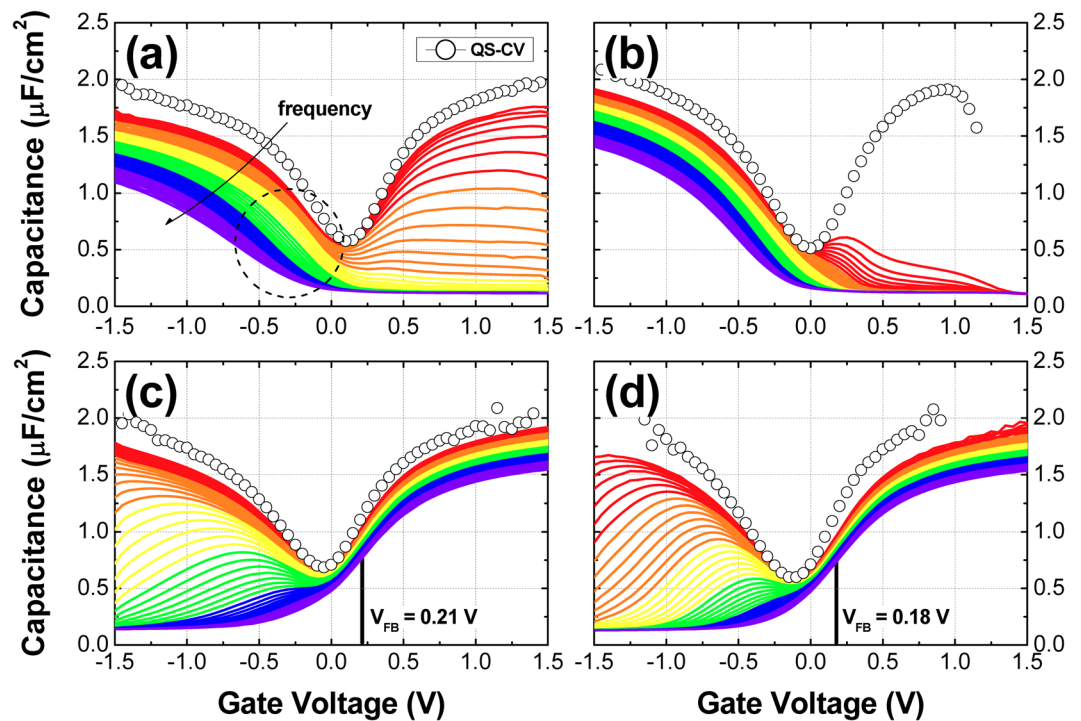


Figure 3. Quasi-static and high-frequency (100 Hz–1 MHz) C – V characteristics of the $\text{HfO}_2/\text{Al}_2\text{O}_3$ dielectrics on (a,b) p-type and (c,d) n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrates after PMA at 400°C for 30 min: (a,c) FGA and (b,d) H_2 -HPA.

was observed on both p- and n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrates (Fig. 3a and c), which indicates the existence of a high density of interface states and the occurrence of strong Fermi-level pinning^{8,29}. For the p-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrate after FGA, a large amount of dispersion at the accumulation region (at a negative bias) was observed. This abnormal C – V behavior can be attributed to border traps⁷ (or disorder-induced gap states³⁰) in the defective near-interface region, probably originating from the wet-chemical cleaning, *ex situ* ALD process, damage that occurred during the electrode deposition, etc²². In addition, the comparison with the n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ sample (Fig. 3c) indicates that a larger number of border traps existed near the valence band (VB) edge of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ than that near the conduction band (CB) edge of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. However, considering the largest dispersion and stretch-out of the frequency-dependent C – V curves near V_{FB} (see the black dashed circle in Fig. 3a), there is also a possibility of an additional strong Fermi-level pinning effect due to the high density of interface states located close to the VB edge of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ band gap. In addition, a systematic increase in the frequency-dependent hump at a gate bias range of -1.5 V to 0 V for the FGA sample on the n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ suggests strong Fermi-level pinning by the high density of interface states. When H_2 -HPA was performed, the observed hump and the stretch-out of the C – V curve were significantly suppressed on both p- and n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrates (see Fig. 3b and d). This improvement suggests effective passivation of the interface states (probably the dangling bonds of the substrate elements) by hydrogen^{7–9}. In addition to the passivation of interface traps, most recently, Tang *et al.* reported a simultaneous reduction in the border trap density for $\text{Al}_2\text{O}_3/\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$ capacitors as a result of FGA⁹. However, this effect was not clearly noticeable in the case of the n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrate when H_2 -HPA was performed, probably due to the larger number of border traps (related to the degree of frequency dispersion in accumulation⁷) created by the existence of a highly defective near-interface region originating from different sample preparation conditions.

To closely observe the effect of H_2 -HPA on the passivation of the interface states, we examined the degree of Fermi-level movement by drawing two-dimensional contour plots of parallel conductance (G_p)^{4,29}, as given in Fig. 4. G_p was determined from the following equation:

$$G_p = \frac{\omega^2 C_{\text{ox}}^2 G_m}{G_m^2 + \omega^2 (C_{\text{ox}} - C_m)^2}, \quad (1)$$

where C_m and G_m are the measured capacitance and conductance, respectively, at different frequencies in the parallel mode, ω is the angular frequency, and C_{ox} is the oxide capacitance^{4,29}. The C_{ox} value was assumed to be the accumulation capacitance determined from the QS C – V curve. The solid trace lines of the peak G_p values in Fig. 4 are indicative of the degree of Fermi-level pinning^{8,29}. When compared to the FGA sample, the H_2 -HPA samples on both p- and n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layers exhibited trace lines with a steeper slope with varying gate voltages, which indicated more alleviated Fermi-level pinning and coincided well with the frequency-dependent C – V behavior shown in Fig. 3. In addition, considering the C – V analysis results shown in Figs 3 and 4, one of the most

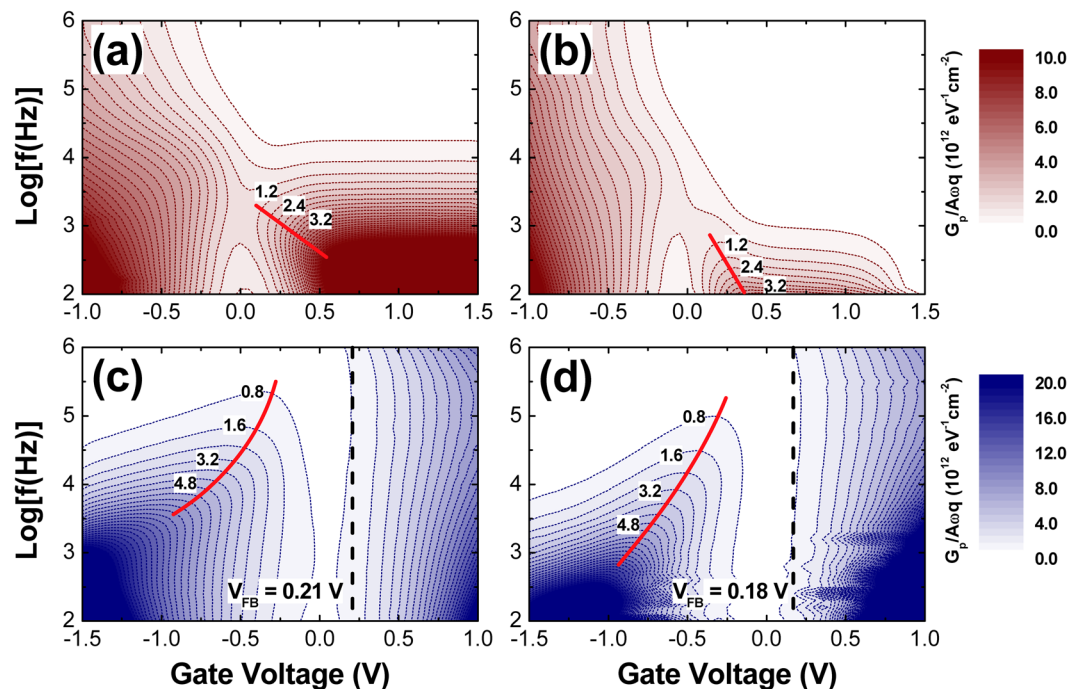


Figure 4. Normalized parallel conductance ($G_p/\omega qA$) as a function of the gate voltage and frequency measured from (a,b) p-type and (c,d) n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors. Here, ω is the measurement angular frequency and A is the capacitor area. The samples were subjected to PMA at 400°C for 30 min: (a,c) FGA and (b,d) H_2 -HPA.

notable results is the much greater effectiveness of H_2 -HPA in suppressing D_{it} in the top half of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ band gap. This is apparent in the much smaller dispersive feature in inversion for the p-type sample (comparing Fig. 3b with Fig. 3a) and in the much steeper trajectory of the normalized G_p (comparing Fig. 4b with Fig. 4a). The improvement in the interface trap response in the bottom half of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ band gap (n-type substrates measured in inversion) for the H_2 -HPA sample is less obvious than in the case of the reference FGA process. Therefore, it seems that H_2 -HPA is good for repairing/passivating the interface traps between the midgap and the CB edge but not for those near the VB edge.

These results suggest that annealing under high-pressure H_2 reduces the density of Ga dangling bonds or anti-site defects at the interface because these defects have transition-state energies centered near the CB edge of GaAs³¹ and may tail into the upper half of the $\text{In}_{1-x}\text{Ga}_x\text{As}$ band gap. Apparently, the annealing is less effective in removing As dangling bonds, which have an energy level near the VB edge³¹. Although the exact reason why it happens this way is not clear yet, there is a possibility that the atomic hydrogen will bind more strongly to group III atoms at the interface, considering that the Pauling electronegativity differences for In–H and Ga–H are larger than those for As–H³². Meanwhile, because In and Ga seem to diffuse into the high- k film much more readily under increased H_2 pressure, this would tend to generate As dangling bonds at the interface region. Therefore, it is possible that more As dangling bonds are passivated by the H_2 -HPA, but more are generated at the same time by In and Ga out-diffusion. Because we do not have a clear picture of exactly which of these two effects (hydrogen passivation versus new dangling bond generation) is most important, these hypotheses should be tested in our future work.

Figure 5 shows the leakage current characteristics of the MOS capacitors on both p- and n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrates, where the gate bias was applied under an electron injection condition from the gate and substrate sides, respectively. Regardless of the substrate doping type, the leakage current increased by approximately one order of magnitude at ± 2.0 V when the H_2 pressure was increased from 0.04 to 30 bar. As evidenced from the chemical analyses results, the incorporation of more In–O/Ga–O bonds and the resulting formation of trap states within the high- k film by the high H_2 pressure may be plausible explanations for the degraded leakage current characteristics.

Conclusion

In summary, we investigated the effects of H_2 -HPA on the out-diffusion of substrate elements and the electrical properties of an ALD- $\text{HfO}_2/\text{Al}_2\text{O}_3$ gate stack on $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ with different doping types. As the H_2 pressure was increased from 0.04 (FGA) to 30 bar (H_2 -HPA) under an identical thermal budget (400°C for 30 min), the out-diffusion of In and Ga elements into the high- k dielectric stack was significantly enhanced. In comparison to conventional FGA, H_2 -HPA significantly alleviated the Fermi-level pinning of the $\text{HfO}_2/\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS capacitors by passivating the interface states; this effect was more pronounced on the p-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ than on the n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. However, when H_2 -HPA was used, the leakage current characteristics were somewhat degraded on both p- and n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrates. This is believed to be affected by the enhanced In/Ga incorporation and the subsequent defect formation within the high- k stack because of the high

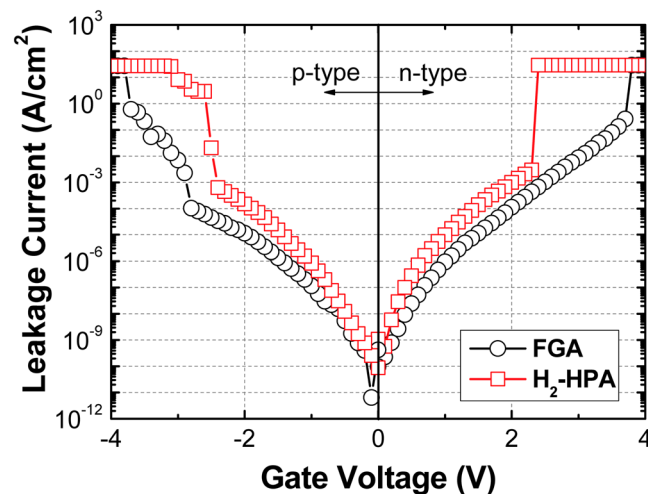


Figure 5. Leakage current density vs. gate voltage for $\text{HfO}_2/\text{Al}_2\text{O}_3$ dielectrics on p- and n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrates after FGA and H_2 -HPA.

Substrates	Layers	Thickness (nm)	x	Dopant	Doping conc. (cm^{-3})
p-type $\text{In}_{1-x}\text{Ga}_x\text{As}$ on p^+ InP	$\text{In}_{1-x}\text{Ga}_x\text{As}$	100	0.53	Be	5×10^{17}
	$\text{In}_{1-x}\text{Ga}_x\text{As}$	150	0.53	Be	1×10^{17}
	p^+ InP	650,000	—	Zn	2×10^{18}
n-type $\text{In}_{1-x}\text{Ga}_x\text{As}$ on n^+ InP	$\text{In}_{1-x}\text{Ga}_x\text{As}$	150	0.53	Si	5×10^{17}
	$\text{In}_{1-x}\text{Ga}_x\text{As}$	100	0.53	Si	1×10^{17}
	n^+ InP	650,000	—	S	3×10^{18}

Table 1. Specifications of the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ wafers used in this experiment.

H_2 pressure. As a result, in the future, optimization of the H_2 pressure will be needed to minimize the degradation of the leakage current characteristics while achieving improved interface properties with $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrates.

Methods

MOS Capacitor Fabrication. MOS capacitors were fabricated on both p- and n-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layers epitaxially grown on InP. The $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InP}$ wafers were supplied by Intelligent Epitaxy Technology, Inc., and their specification is provided in Table 1. Before the high- k gate dielectric deposition, the cleaved substrates were cleaned using a 10% HCl aqueous solution for 30 s. A stacked high- k dielectric of 4.5 nm $\text{HfO}_2/1.0$ nm Al_2O_3 was deposited *in situ* using trimethylaluminum (TMA)– H_2O and tetrakis(ethylmethylamino)hafnium (TEMAHf)– H_2O precursor combinations at 200 °C. The prepared films followed a gate metallization step, *i.e.*, a lift-off process using a sputter-deposited TaN (50 nm) electrode with a Ni (10 nm) capping layer. Afterwards, conventional FGA and H_2 -HPA were performed at 400 °C for 30 min prior to the electrical characterization. The FGA was performed at atmospheric pressure using 4% H_2 gas balanced with N_2 , which corresponds to a H_2 partial pressure of 0.04 bar. For H_2 -HPA, 100% H_2 was used at a high pressure of 30 bar.

Measurement and Characterization. For the electrical characterization of the fabricated MOS capacitors, an Agilent E4980A LCR meter, an Agilent B1500A semiconductor device analyzer, and Keithley 6514 electrometer/230 programmable voltage source were used. In addition, the compositional change in the high- k films induced by different PMA conditions were probed by ToF-SIMS (TOF-SIMS 5, ION-TOF), and ARXPS (K-alpha, Thermo Scientific Inc.) with an Al K_α (1486.6 eV) source. For the ARXPS measurement, the take-off angle was varied from 20° to 90°, and a pass energy of 20 eV was used.

References

- Oktyabrsky, S. & Ye, P. D. Fundamentals of III-V semiconductor MOSFETs. *Springer New York*. (173–181 (2010)).
- del Alamo, J. A. Nanometre-scale electronics with III-V compound semiconductors. *Nature* **479**, 317–323 (2011).
- Takagi, S. *et al.* III-V/Ge channel MOS device technologies in nano CMOS era. *Jpn. J. Appl. Phys.* **54**, 06FA01 (2015).
- Nicollian, E. H. & Brews, J. R. MOS (Metal Oxide Semiconductor) physics and technology. *John Wiley & Sons, Inc. New York*. 212–221, 782–785 (1982).
- Himpel, F. J. *et al.* Microscopic structure of the SiO_2/Si interface. *Phys. Rev. B* **38**, 6084–6096 (1988).
- Cartier, E., Stathis, J. H. & Buchanan, D. A. Passivation and depassivation of silicon dangling bonds at the Si/SiO_2 interface by atomic hydrogen. *Appl. Phys. Lett.* **63**, 1510 (1993).
- Kim, E. J. *et al.* Border traps in $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (100) gate stacks and their passivation by hydrogen anneals. *Appl. Phys. Lett.* **96**, 012906 (2010).

8. Hwang, Y., Engel-Herbert, R., Rudawski, N. G. & Stemmer, S. Effect of postdeposition anneals on the fermi level response of $\text{HfO}_2/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ gate stacks. *J. Appl. Phys.* **108**, 034111 (2010).
9. Tang, K. *et al.* Interface defect hydrogen depassivation and capacitance-voltage hysteresis of $\text{Al}_2\text{O}_3/\text{InGaAs}$ gate stacks. *ACS Appl. Mater. Interfaces* **9**, 7819–7825 (2017).
10. Kim, T.-W. *et al.* Impact of H_2 high-pressure annealing onto InGaAs quantum-well metal-oxide-semiconductor field-effect transistors with $\text{Al}_2\text{O}_3/\text{HfO}_2$ gate-stack. *IEEE Electron Device Lett.* **36**, 672–674 (2015).
11. Jeon, S. *et al.* Triple high k stacks ($\text{Al}_2\text{O}_3/\text{HfO}_2/\text{Al}_2\text{O}_3$) with high pressure (10 atm) H_2 and D_2 annealing for SONOS type flash memory device applications. *IEEE Conf. Nanotechnol.* **4th**, 53–55 (2004).
12. Park, H. *et al.* Improved interface quality and charge-trapping characteristics of MOSFETs with high- k gate dielectric. *IEEE Electron Device Lett.* **26**, 725–727 (2005).
13. Akbar, M. S. *et al.* Improvement in bias instabilities of Hf-silicate by dilute hydrochloric acid (500:1) post-deposition rinsing and its effect after high-pressure H_2 Anneal. *Appl. Phys. Lett.* **87**, 252903 (2005).
14. Krylov, I., Gavrilov, A., Eizenberg, M. & Ritter, D. Indium outdiffusion and leakage degradation in metal/ $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ capacitors. *Appl. Phys. Lett.* **103**, 053502 (2013).
15. Krylov, I., Winter, R., Ritter, D. & Eizenberg, M. Indium out-diffusion in $\text{Al}_2\text{O}_3/\text{InGaAs}$ stacks during anneal at different ambient conditions. *Appl. Phys. Lett.* **104**, 243504 (2014).
16. Weiland, C. *et al.* Hard X-ray photoelectron spectroscopy study of As and Ga out-diffusion in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{Al}_2\text{O}_3$ film systems. *Appl. Phys. Lett.* **101**, 061602 (2012).
17. Sanchez-Martinez, A. *et al.* Diffusion of In and Ga in $\text{TiN}/\text{HfO}_2/\text{InGaAs}$ nanofilms. *J. Appl. Phys.* **114**, 143504 (2013).
18. Cabrera, W. *et al.* Diffusion of $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ elements through hafnium oxide during post deposition annealing. *Appl. Phys. Lett.* **104**, 011601 (2014).
19. An, C.-H., Mahata, C., Byun, Y.-C. & Kim, H. Atomic-layer-deposited $(\text{HfO}_2)_{1-x}(\text{Al}_2\text{O}_3)_x$ nanolaminate films on InP with different Al_2O_3 contents. *J. Phys. D: Appl. Phys.* **46**, 275301 (2013).
20. Kang, Y.-S. *et al.* Structural evolution and the control of defects in atomic layer deposited $\text{HfO}_2\text{-Al}_2\text{O}_3$ stacked films on GaAs . *ACS Appl. Mater. Interfaces* **5**, 1982–1989 (2013).
21. Suzuki, R. *et al.* Impact of atomic layer deposition temperature on $\text{HfO}_2/\text{InGaAs}$ metal-oxide-semiconductor interface properties. *J. Appl. Phys.* **112**, 084103 (2012).
22. Tang, K., Meng, A. C., Droopad, R. & McIntyre, P. C. Temperature dependent border trap response produced by a defective interfacial oxide layer in $\text{Al}_2\text{O}_3/\text{InGaAs}$ gate stacks. *ACS Appl. Mater. Interfaces* **8**, 30601–30607 (2016).
23. Kim, E. J. *et al.* Atomically abrupt and unpinned $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ interfaces: experiment and simulation. *J. Appl. Phys.* **106**, 124508 (2009).
24. Aguirre-Tostado, F. S. *et al.* Indium stability on InGaAs during atomic H surface cleaning. *Appl. Phys. Lett.* **92**, 171906 (2008).
25. Yamada, M. GaOH : unstable species liberated from GaAs surface oxides during atomic hydrogen cleaning. *Jpn. J. Appl. Phys.* **35**, L651–L653 (1996).
26. Yamada, M., Ide, Y. & Tone, K. Effect of atomic hydrogen on GaAs (001) surface oxide studied by temperature-programmed desorption. *Jpn. J. Appl. Phys.* **31**, L1157–L1160 (1992).
27. Piskorski, K. & Przewlocki, H. M. The methods to determine flat-band voltage V_{FB} in semiconductor of a MOS structure, *The 33rd International Convention MIPRO*, 37–42 (2010).
28. Winter, R., Ahn, J., McIntyre, P. C. & Eizenberg, M. New method for determining flat-band voltage in high mobility semiconductors. *J. Vac. Sci. Technol. B* **31**, 030604 (2013).
29. Engel-Herbert, R., Hwang, Y. & Stemmer, S. Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces. *J. Appl. Phys.* **108**, 124101 (2010).
30. Galatage, R. V. *et al.* Accumulation capacitance frequency dispersion of III-V metal-insulator-semiconductor devices due to disorder induced gap states. *J. Appl. Phys.* **116**, 014504 (2014).
31. Robertson, J. Model of interface states at III-V oxide interfaces. *Appl. Phys. Lett.* **94**, 152104 (2009).
32. Allred, A. L. Electronegativity values from thermochemical data. *J. Inorg. Nucl. Chem.* **17**, 215–221 (1961).

Acknowledgements

This work was supported by the Samsung Electronics' University R&D program (SR170407_0001) and also by the Future Semiconductor Device Technology Development Program (Grant No. 10045216) funded by MOTIE (Ministry of Trade, Industry & Energy) and KSRC (Korea Semiconductor Research Consortium).

Author Contributions

S.C. was the initiator of this work and conducted most of the experiments. Y.A., C.L., and J.S. helped in conducting ALD, capacitor fabrication, and electrical characterization. M.-C.N. conducted a H_2 -HPA experiment. Y.-C.B., R.C., and P.C.M. discussed the results and provided helpful insights to prepare the manuscript. S.C. and H.K. co-wrote the manuscript. All authors discussed the results and reviewed the manuscript.

Additional Information

Supplementary information accompanies this paper at doi:10.1038/s41598-017-09888-6

Competing Interests: The authors declare that they have no competing interests.

Publisher's note: Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.



Open Access This article is licensed under a Creative Commons Attribution 4.0 International License, which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons license, and indicate if changes were made. The images or other third party material in this article are included in the article's Creative Commons license, unless indicated otherwise in a credit line to the material. If material is not included in the article's Creative Commons license and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder. To view a copy of this license, visit <http://creativecommons.org/licenses/by/4.0/>.

© The Author(s) 2017