Towards systems-on-a-chip

Progress in silicon photonics is delivering chips that can densely pack photonics and electronics together and perform multidimensional quantum information processing.

The level of sophistication of photonic integration within silicon chips has reached new heights with the recent publication of several high-profile papers on the topic. In mid-April, two papers appeared in *Nature* and *Science* almost simultaneously, reporting the dense integration of photonics with silicon nanoelectronics on a bulk complementary metal-oxide–semiconductor (CMOS) chip[1] and the fabrication of a large-scale silicon photonics quantum circuit[2], respectively. The achievements collectively demonstrate the great strides that are being made in the evolution of silicon photonics and photonic integration towards the goal of realizing powerful systems-on-a-chip.

The electronic–photonic silicon chip reported in *Nature* was designed by a US collaboration from the Massachusetts Institute of Technology (MIT), University of California at Berkeley, University of Colorado, Boston University and the State University of New York. It provides monolithic integration of photonic components such as optical waveguides, micro-ring modulators, grating couplers and avalanche photodetectors into a CMOS chip containing analog and digital electronics (Fig. 1a). The optical components are made by using a carefully optimized thin layer of polycrystalline silicon (~200 nm thick) deposited on islands of silicon oxide inside trenches within the bulk CMOS chip.

To date, silicon photonic chips have strongly relied on the use of special silicon-on-insulator (SOI) wafers rather than the standard silicon wafers used by CMOS microelectronics. In many ways, this works well and sophisticated optical chips have been made using SOI wafers, but they are expensive with a less well-developed supply chain. In contrast, bulk silicon wafers used in CMOS processes are ubiquitous and low cost. Thus, finding a way of integrating photonics into standard CMOS wafers is highly attractive.

"The key motivation for us is to solve the input/output (I/O) bandwidth limitation of computing chips — both the processor and memory. High-performance logic chips today have massive processing power (many teraFLOPs per second), but their communication to the memory is limited by the bandwidth of electrical I/O," explained Amir Atabaki, a researcher from MIT and the lead author on the *Nature* paper. "Our goal is to replace the electrical I/O with optical I/O with much higher bandwidth and lower power consumption. To be able to do that, we need to integrate optical interconnects with logic and memory chips, which today are all manufactured on bulk silicon wafers."

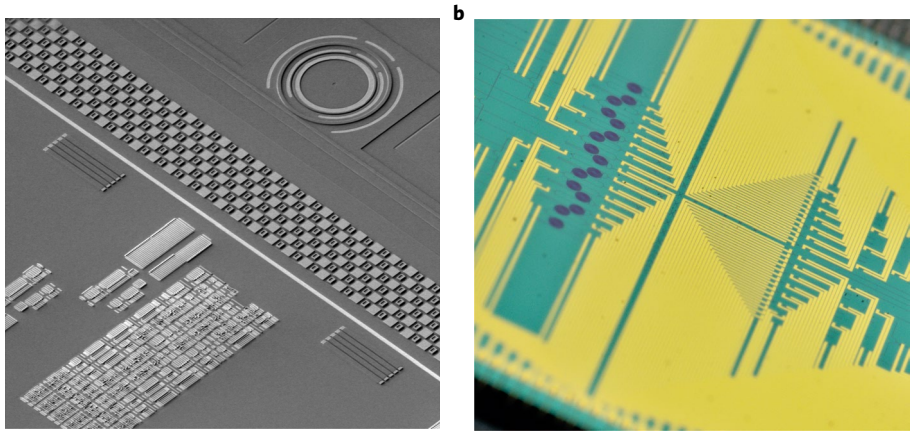

Fig. 1 | Systems-on-a-chip. a, Electronic–photonic silicon chip. **b**, Quantum silicon chip. Figure reproduced from: **a**, ref. [1], Macmillan Publishers Ltd; **b**, ref. [2], AAAS.

The team used their electronic–photonic integration approach to create high-speed photonic transceiver chipsets in CMOS for wavelength-division-multiplexed (WDM) optical communications systems. Each chipset featured four WDM transmitters and receivers operating at a data rate of 10 Gb s^{-1} and consuming just 110 fJ per bit and 500 fJ per bit, respectively. If incorporated into CMOS chips with sub-10 nm node transistor technology that approach would lead to a bandwidth density of >Tb s^{-1} mm^{-2}. Atabaki says that the two biggest challenges were to first find a processing recipe for the polysilicon film so that it had both good optical and electrical properties, and second to incur minimum changes to the CMOS process to avoid any degradation to the nanoscale transistors on the chips.

As for the quantum silicon chip reported in *Science*, this was the result of a collaboration of scientists from the UK, China, Denmark, Spain, Germany and Poland. In particular, researchers from the University of Bristol, Peking University, Technical University of Denmark, University of Copenhagen, the ICFO and ICREA institutes in Barcelona, Max Planck Institute for Quantum Optics and the Polish Academy of Sciences all played a role.

The chip, made by electron-beam lithography, enables on-chip generation and manipulation of multidimensional entangled quantum states, which have potential applications in more efficient quantum communications and information processing. Approximately 550 photonic components are monolithically integrated on a single chip including: 16 photon sources that use spontaneous four-wave mixing to generate photon pairs in superposition across 16 optical modes; 93 thermo-optic phase shifters; 122 multimode interferometer beamsplitters; 256 waveguide crossers and 64 grating couplers (Fig. 1b). After passing through the chip, photons are coupled into optical fibres by means of the grating couplers and passed to superconducting nanowire detectors.

The scientists involved in the work are confident that the approach can be scaled further in terms of device count and integration. "The current devices are far from the limits that can be reached using silicon photonics," commented Mark Thompson from the University of Bristol. "Utilizing state-of-the-art 300-mm-deep UV immersion lithography could lead to significant improvements in component performance, yield and scalability — with 100,000-component devices not an unrealistic target." ❐

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References
1. Atabaki, A. H. et al. *Nature* **556**, 349–354 (2018).
2. Wang, J. et al. *Science* **360**, 285–291 (2018).