2D MATERIALS

A longer-lasting memory in layered semiconductors

A volatile memory built by assembly of layered semiconductors into a van der Waals heterostructure gives longer refresh times and an opportunity to improve energy efficiency.

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The evolution of electronics is largely driven by energy efficiency, from the adoption of solid-state devices in lieu of vacuum tubes, to the reduction of wiring length via transistor integration into a single substrate, to the myriad advances in solid-state device technology that have followed thereafter. The energy efficiency of electronics has spurred numerous fundamental works[1,2], and the quest for low-power devices is as important today as ever[3] with the ubiquitous presence of electronics in modern life.

Now, writing in *Nature Nanotechnology*, Liu et al.[4] report an energy-efficient memory composed of a van der Waals heterostructure with a short write time and a long refresh time that the authors refer to as a quasi-non-volatile memory. The work strikes a fine balance between the energy efficiency of non-volatile memory and the speed of volatile memory. Once information is written into an ideal non-volatile memory, no further energy is consumed. However, this stability typically comes at the cost of a long writing time. Engravings in stone steles are a fine example of a reliable, non-volatile memory. In contrast, a volatile memory is designed for fast writing speed but must be periodically refreshed. Each refresh operation costs energy, and the challenge therefore is to achieve a long time between refresh operations without incurring the cost of an unduly long writing time.

In a tour de force of van der Waals heterostructure assembly, Liu et al. have fabricated heterostructures made of two-dimensional HfS_2, MoS_2, WSe_2 and hBN flakes to create memory cells with a semi-floating gate transistor architecture[5]. The core of the structure is a field effect transistor with a semiconducting HfS_2 layer, WSe_2 channel and a highly insulating hBN gate dielectric. The semiconducting HfS_2 layer acts as a floating gate, storing the charge that corresponds to either a logical state 0 or logical state 1 (Fig. 1). Read-out of the memory cell is achieved through the shift in the threshold voltage of the WSe_2–hBN transistor, which is induced by the charge stored on the HfS_2 floating gate. Writing to the memory cell is achieved by injecting charge to the floating gate through a WSe_2–MoS_2 heterojunction that acts as a van der Waals diode. Charge can be injected under forward bias during the write operation, and charge leakage from the HfS_2 is reduced to a mere trickle under reverse bias.

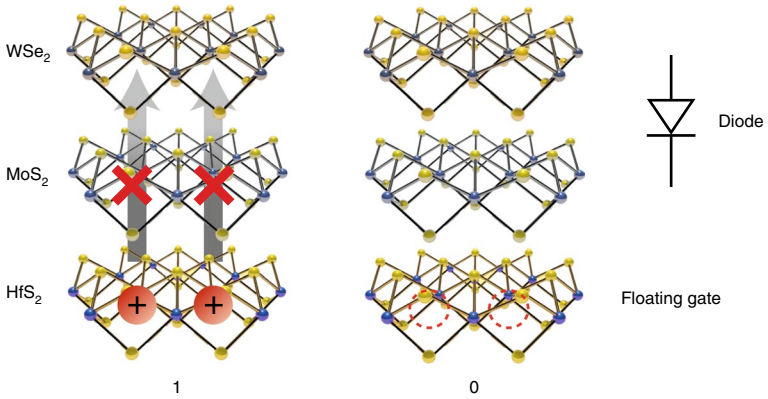

Fig. 1 | The floating gate memory of Liu et al. consists of a van der Waals heterostructure with WSe_2, MoS_2 and HfS_2 layers. The HfS_2 is the floating gate that stores the excess positive charge corresponding to a logical 1 state, while the absence of excess positive charge corresponds to a logical 0 state. The long refresh time arises from the diode action of the MoS_2/WSe_2 layers, reducing the leakage of charge from the floating gate down to a trickle.

The presented quasi-non-volatile memory was shown to have a refresh time of 10 ms, more than 150 times longer than a typical refresh time of dynamic random access memory essential to computer cores. The write time of the memory of Liu et al. is nonetheless comparable to the typical 10 ns write time of dynamic random access memory. This feat was achieved through exquisite voltage control of the charge carrier confinement in van der Waals heterostructures.

The work serves as a demonstration of the versatility and utility of van der Waals heterostructures. There are hundreds of experimentally known layered materials[6,7], with a recent theoretical study[8] suggesting that there are over 1,000 layered materials that can be easily exfoliated. This opens a vast design space for van der Waals heterostructures, which researchers have only begun to map out.

Looking to the future, the most daunting challenge to the adoption of van der Waals heterostructures in the electronics industry is the development of methods for wafer-scale synthesis. Artisanal, manual assembly of heterostructures has enabled demonstration of the quasi-non-volatile memory. Bringing this work out of the laboratory and into next-generation, energy-efficient electronics requires significant advances in the manufacture of van der Waals heterostructures. ❐

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