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Charge carrier modulation in graphene on ferroelectric single-crystal substrates

Nahee Park¹, Hyunkyung Lee², Jeongmin Park¹, Tuan Khanh Chau¹, Hojin Kang¹, Haeyong Kang¹  and Dongseok Suh¹ 

Abstract

Charge carrier modulation of graphene using the ferroelectricity of a nearby dielectric can be useful for controlling the electronic properties of graphene. However, when graphene is located on ferroelectric oxides, their electrical coupling frequently shows abnormal behaviors, such as anti-hysteresis, in field-effect transistor operation. From the systematic examination of graphene on a ferroelectric oxide single-crystal $[\text{Pb}(\text{Mg}_{1/3}\text{Nb}_{2/3})\text{O}_3]_{1-x}-[\text{PbTiO}_3]_x$ (PMNPT) substrate, we observed that the ferroelectric modulation of graphene was significantly influenced by the ambipolar nature of graphene and ferroelectric-assisted charge trapping with carrier-type dependency. For graphene/hexagonal-BN on the PMNPT, the Coulomb interaction between charges in interfacial traps and ferroelectric polarization seems to decouple the graphene conductance from the polarization field and induce only the charge trap effect on device performance. Consequently, the asymmetric surface charge compensation of ferroelectric oxide by the ambipolar graphene channel determines the detailed coupling process between the charge carrier of graphene and ferroelectric polarization, resulting in direct ferroelectric coupling or indirect anti-hysteretic coupling.

Introduction

Ferroelectricity is one of the most basic phenomena frequently observed in functional dielectric materials. The broken crystal inversion symmetry induces a permanent electric dipole moment inside a material, and this spontaneous polarization is an extensively studied topic in solid-state physics^{1–3}. The polarization state can be manipulated using an external electric field, and its hysteresis is shown in the electric-field-dependent polarization curve. Ferroelectric materials can be used in field-effect transistors, where a ferroelectric layer functions as a gate dielectric insulator. The charge carrier modulation of the conducting channel is performed using the ferroelectric polarization field. From its nonvolatility, the information can be stored in the form of the polarization

direction. This can be monitored using the magnitude change in the source-drain current that flows through the channel of the semiconducting material in contact with the ferroelectric gate dielectric layer^{4,5}. There have been several combinations of ferroelectric and semiconducting materials, such as $\text{Pb}(\text{Zr,Ti})\text{O}_3$ on silicon and polyvinylidene-fluoride/organic-semiconductors, which have been successfully operated as ferroelectric-gated field-effect transistors^{6–16}.

Unlike traditional semiconductors, atomically thin two-dimensional (2D) materials such as graphene have been employed as a conducting channel owing to their metallic charge carrier modulation capability^{17–45}. Especially for graphene, a Dirac-cone-shaped band structure enables easy control of the chemical potential by the permanent electric dipole moment of a ferroelectric layer. As expected, the conductance of graphene in contact with ferroelectric polymers has been reported to show direct coupling between the charge carriers of graphene and ferroelectric polarization^{17–23}. Interestingly, however, many researchers have also reported anti-hysteresis

Correspondence: Haeyong Kang (haeyong.kang@pusan.ac.kr) or Dongseok Suh (energy.suh@skku.edu)

¹Department of Energy Science, Sungkyunkwan University, Suwon 16419, Republic of Korea

²Department of Physics, Pusan National University, Busan 46241, Republic of Korea

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behavior, whose hysteresis direction is opposite to that of the normal ferroelectric hysteresis curve, especially when a ferroelectric oxide material is used as a back-gate dielectric for graphene transistors^{24–35}. In addition, in some reports, the shape of conductance hysteresis varies as a function of temperature or applied electric field^{27,30,33,36–38}. Such diversity in the shape of hysteresis curves in graphene/ferroelectric systems indicates that the interface between the two materials is critical to determining the coupling of charges between graphene and the ferroelectric layer. Nonetheless, this behavior is not completely understood despite the simplicity of the device structure.

When mechanical contact between a ferroelectric oxide and graphene is considered, the van der Waals interaction is the only driving force for their contact. Therefore, the adhesion and/or spacing between the ferroelectric oxide and graphene is critically important. At first glance, the pure ferroelectric polarization field is expected to induce charges inside graphene and/or interfacial charge traps that act as extrinsic doping sources. From this aspect, an emphasis has been placed on the role of interfacial molecules that are trapped between graphene and ferroelectric oxide, as the characteristics of these molecules seem to determine the type of interaction between graphene and ferroelectrics. However, these molecules are still insufficient to explain the variety of charge trapping phenomena associated with ferroelectrics^{46–52}. In this study, we report the systematic analysis of graphene-ferroelectric devices, in which $[\text{Pb}(\text{Mg}_{1/3}\text{Nb}_{2/3}\text{O}_3)_{1-x}[\text{PbTiO}_3]_x$ (PMNPT) is used as the ferroelectric oxide layer. Due to the single-crystalline feature of the PMNPT, we can sharply define the motion of polarization switching. Furthermore, the ambipolar charge conduction behavior of graphene in response to the applied electric field can be sensitively monitored by tracing the movement of the charge neutrality point (CNP). Using field-effect devices consisting of graphene and PMNPT, the unconventional charge coupling phenomena between graphene and ferroelectric oxide are carefully analyzed.

Methods

Experimental design and device fabrication

We designed and investigated two types of graphene devices in the configuration of a back-gated transistor, where a 100- μm -thick ferroelectric single-crystal PMNPT oriented along the (001) direction substrate (IBULE Photonics, Republic of Korea) was employed as a back-gate dielectric layer. For one type, there was direct contact between graphene and PMNPT, while the other type included a hexagonal boron nitride (*h*BN) layer between graphene and PMNPT, which provides an atomically flat surface for graphene. The illustrations of the basic devices are depicted in Fig. 1a, b.

After mechanically exfoliating the graphene layer on a polymethyl methacrylate (PMMA)-coated silicon substrate and the *h*BN layer (HQ Graphene, Netherlands) on a PMNPT substrate, the graphene was transferred onto the flat surface area of PMNPT (see details in Figs. S1, S2 in the Supplementary Information (SI)) or onto *h*BN/PMNPT by using the dry-transfer method. Standard e-beam lithography was used to form the source and drain electrodes with Au/Cr bimetal layers.

Fabricated device inspection

The top-view optical images of both fabricated devices are depicted in Fig. 1c, d. The layer numbers of exfoliated graphene samples were estimated from the Raman spectra (Renishaw Raman, UK), which confirmed that all the graphene flakes were monolayers (Fig. S3 in SI). The thickness of the *h*BN layer was approximately 30 nm, as depicted in Fig. 1e, which was measured by the tapping mode of the atomic force microscope (AFM) instrument (Hitachi High-tech, Japan). The surface topography and ferroelectric domain of PMNPT were obtained simultaneously using the AFM instrument NX10 (Park systems, Republic of Korea).

Electrical characterization

The electrical transport was measured inside the Physical Property Measurement System (PPMS, Quantum Design Inc., USA) using an Agilent B1500A (Keysight, USA). The standard electrical measurement setup for three-terminal back-gated field-effect transistors was configured, as shown in Fig. 1f. The standard procedures for the device operation are described as follows. For V_G sweeps within a specific range, V_G starts from 0 V and increases to a positive maximum. Then, V_G decreases from that positive maximum to the negative maximum. Finally, V_G moves again from that negative maximum to 0 V. During the sweep, V_G varies continuously without breaking. More specifically, in Fig. 2, the right arrow in the legend box corresponds to an increasing V_G from the negative maximum to 0 V and from 0 V to the positive maximum, while the left arrow corresponds to the movement of V_G from positive to negative.

Analysis framework for hysteretic charge conduction in graphene devices

Various hysteresis curves, frequently observed in many electrical transport experiments of graphene field-effect transistors, can be understood systematically in the framework introduced in Fig. 1g. If an insulator such as SiO_2 was employed as a gate dielectric, (in other words, when PMNPT was replaced with SiO_2 in Fig. 1f), then the drain current (I_D) versus the gate voltage (V_G), *i.e.*, the I_D - V_G plot, depicts a typical V-shaped curve, as shown in Fig. 1g (i), where zero conductance at zero gate voltage was expected owing to graphene's intrinsic Dirac-cone band

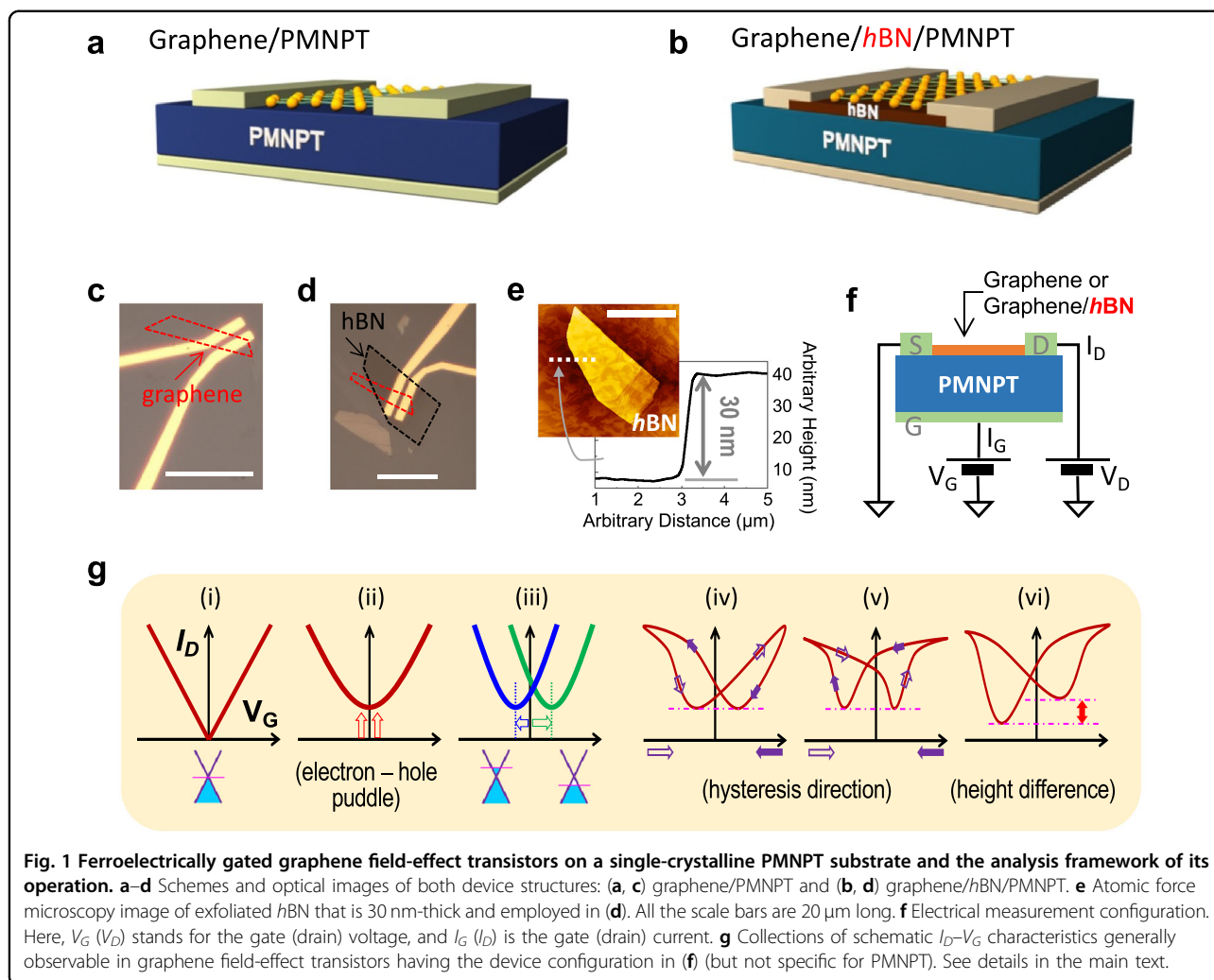


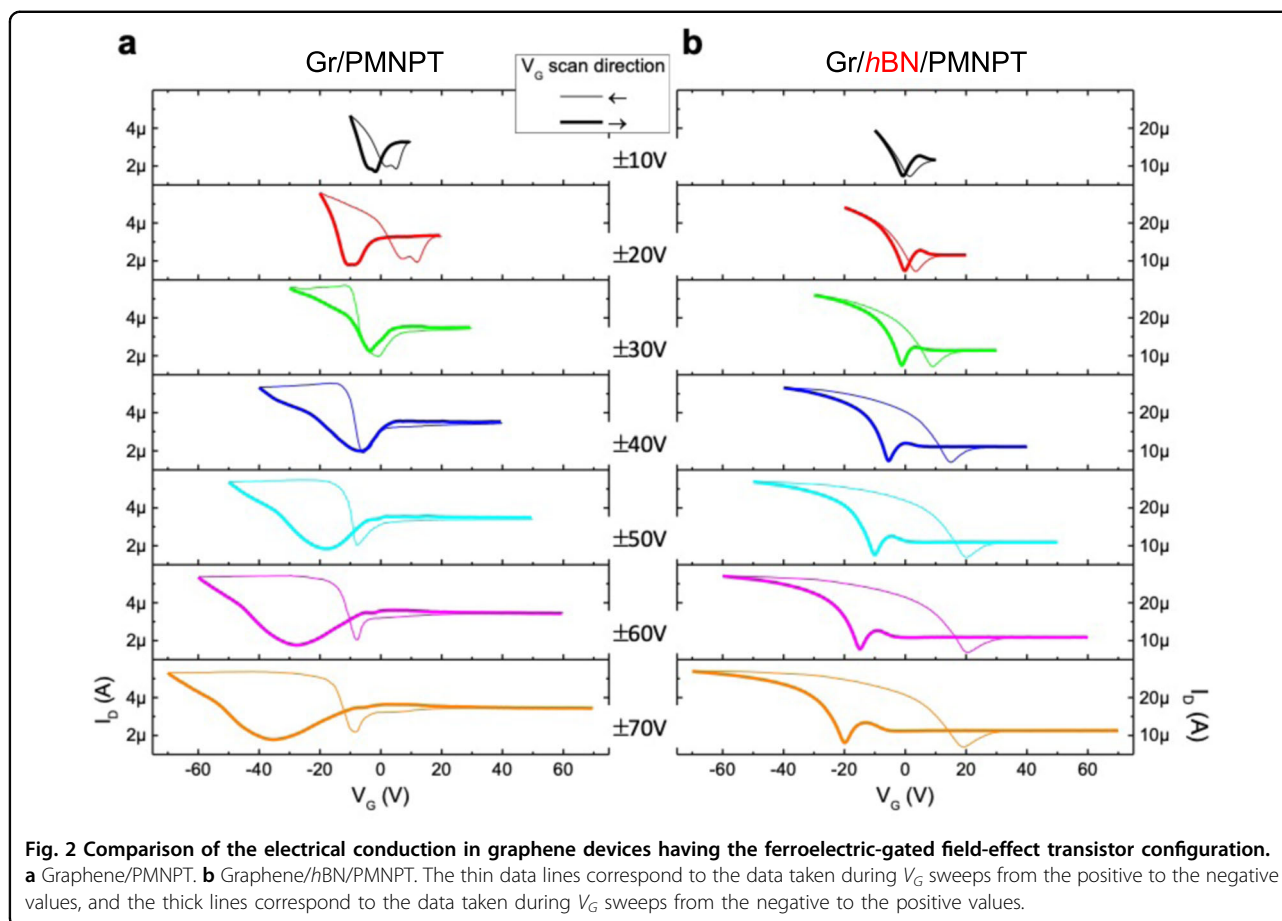
Fig. 1 Ferroelectrically gated graphene field-effect transistors on a single-crystalline PMNPT substrate and the analysis framework of its operation. **a–d** Schemes and optical images of both device structures: **(a, c)** graphene/PMNPT and **(b, d)** graphene/hBN/PMNPT. **e** Atomic force microscopy image of exfoliated hBN that is 30 nm-thick and employed in **(d)**. All the scale bars are 20 μm long. **f** Electrical measurement configuration. Here, V_G (V_D) stands for the gate (drain) voltage, and I_G (I_D) is the gate (drain) current. **g** Collections of schematic I_D – V_G characteristics generally observable in graphene field-effect transistors having the device configuration in **(f)** (but not specific for PMNPT). See details in the main text.

structure, in an ideal case. However, electron-hole puddles are inevitably formed in real samples with spatial inhomogeneity⁵³. Therefore, the minimum conductance is generally not zero, but a finite value exists at the charge neutrality point (CNP), as shown in Fig. 1g (ii). In addition, imperfections such as defects, impurities, or unintentional doping during device fabrication processes can also move CNPs to the left (electron doping) or to the right (hole doping), depending on the chemical potential shift in Fig. 1g (iii).

When I_D – V_G data curves are experimentally obtained during V_G sweeps, various hysteretic conductances can appear, as shown in Fig. 1g (iv–vi), with different hysteresis directions and mixtures of many complicated behaviors. For a clear understanding, careful analysis between charge trap phenomena and the characteristics of gate dielectrics is needed. In this work, a ferroelectric single-crystal PMNPT was used as a gate dielectric, and the effect of ferroelectricity on the charge conduction of graphene was intensively studied.

Results and discussion

Figure 2 presents the I_D – V_G curves for graphene-ferroelectric transistors with a graphene/PMNPT structure and that of graphene/hBN/PMNPT at different V_G sweep ranges from ± 10 to ± 70 V with a 10-V interval. For the graphene/PMNPT sample in Fig. 2a, the I_D – V_G curves in the small V_G sweep range depend on the initial polarization states of the PMNPT substrate, which were not well identified. However, as the V_G sweep range increases to cover the coercive voltage of the PMNPT substrate, clear hysteretic I_D – V_G curves appear with ferroelectric switching, and considerably asymmetric shapes of I_D – V_G curves are obtained for this graphene/PMNPT sample⁵⁴. In detail, the V_G sweep from a positive maximum to a negative maximum gives a sharp transition from n - to p -type carrier conversion in the narrow V_G range (approximately between -10 V and 0 V) near the CNP located in the negative V_G region. However, a V_G sweep in the opposite direction, *i.e.*, from a negative maximum to a positive maximum, gives the I_D variation in a much broader V_G range.



On the other hand, in Fig. 2b, the I_D - V_G curves of the graphene/hBN/PMNPT sample show a hysteretic V-shaped conductance variation with respect to V_G . Two clearly separated CNPs, each of which corresponds to the opposite V_G sweep directions, indicate that the effect of ferroelectric switching in PMNPT significantly affects the charge conduction through graphene. However, it is intriguing to note that the hysteresis direction is not the same as what is expected in the conventional ferroelectric field-effect transistor, but it seems to be related to conventional charge trap memory behavior (as in Fig. 1g (iv, v))^{55,56}. One additional consideration is that the I_D - V_G curves in a positive V_G region with electron majority carriers do not show a continuous I_D increase with increasing V_G but anomalously exhibit complete saturation in both the graphene/PMNPT and graphene/hBN/PMNPT cases.

The I_D - V_G curves for the graphene/PMNPT sample in Fig. 2a are analyzed in Fig. 3. From the device structure of the ferroelectric field-effect transistor, the gate current (I_G) passing through the ferroelectric substrate shows a peak when ferroelectric switching occurs during the V_G sweep^{29,33}. Fig. 3a shows the collection of I_G - V_G curves and that of the corresponding I_D - V_G curves taken from Fig. 2a for the V_G scans from positive to negative. In the

top panel, the I_G peak positions are almost the same for all different V_G sweeps, representing the ferroelectric switching of the PMNPT substrate^{29,33}. This clearly implies that when V_G moves from positive to negative values, normal ferroelectric switching occurs irrespective of the V_G sweep range. Additionally, in the bottom panel, the sudden increase in I_D after passing CNP indicates that the majority carriers rapidly change from electrons to holes in the graphene channel (which is schematically illustrated in Figure S4 in SI).

However, for the V_G sweep from negative maximum to positive, as depicted in Fig. 3b, the I_D decreases immediately after the V_G sweep direction changes. This observation deviates from the expectation that the strong ferroelectric polarization field would freeze the carrier density in graphene. Another noticeable feature is that the I_D shows a complete saturation behavior when V_G passes the ferroelectric switching region, as shown in Fig. 2b. It is remarkable that I_D does not move at all inside the dash-dotted square box in Fig. 3b, where the I_G peaks appear clearly. This surely indicates that the ferroelectricity in PMNPT is decoupled from charge conduction in graphene during the V_G sweep from negative maximum to positive.

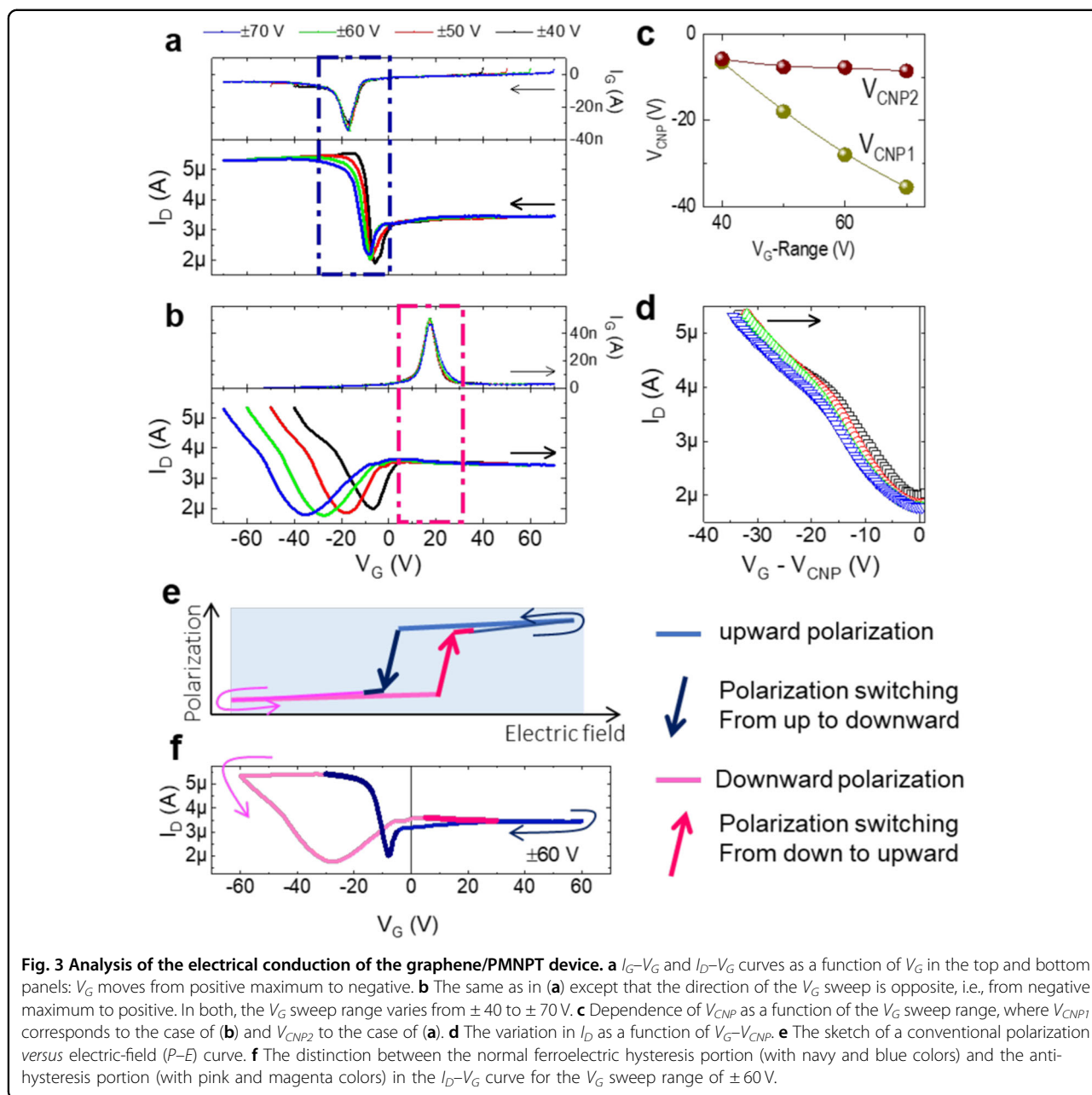


Figure 3c shows the CNP movement as a function of the V_G sweep range. It is noticeable that the position of CNP1 (i.e., V_{CNP1} defined as the CNP during the V_G sweep from a negative maximum to a positive maximum corresponding to Fig. 3b) changes considerably, but that of CNP2 (i.e., V_{CNP2} in the opposite V_G sweep direction corresponding to Fig. 3a) does not change substantially. Because ferroelectric switching is independent of the V_G sweep range only if V_G is larger than the coercive voltage, CNP2 and the results in Fig. 3a can be closely related to the result of direct ferroelectric coupling between graphene and PMNPT. However, the sensitivity of CNP1 to

variations in the V_G sweep range may not be primarily governed by ferroelectricity, but other mechanisms, such as charge trapping, play an important role.

In addition, parts of the data curves in the hole majority (p -type) region in Fig. 3b are taken and plotted as a function of $V_G - V_{CNP1}$ in Fig. 3d. These parts are considerably similar to each other, indicating that the conductance variation in the hole-majority region is almost the same, irrespective of the V_G sweep range. However, the position of CNP1 only shifts linearly according to the negative maximum V_G values, as shown in Fig. 3c. Such results suggest the plausibility of the trapped holes, which

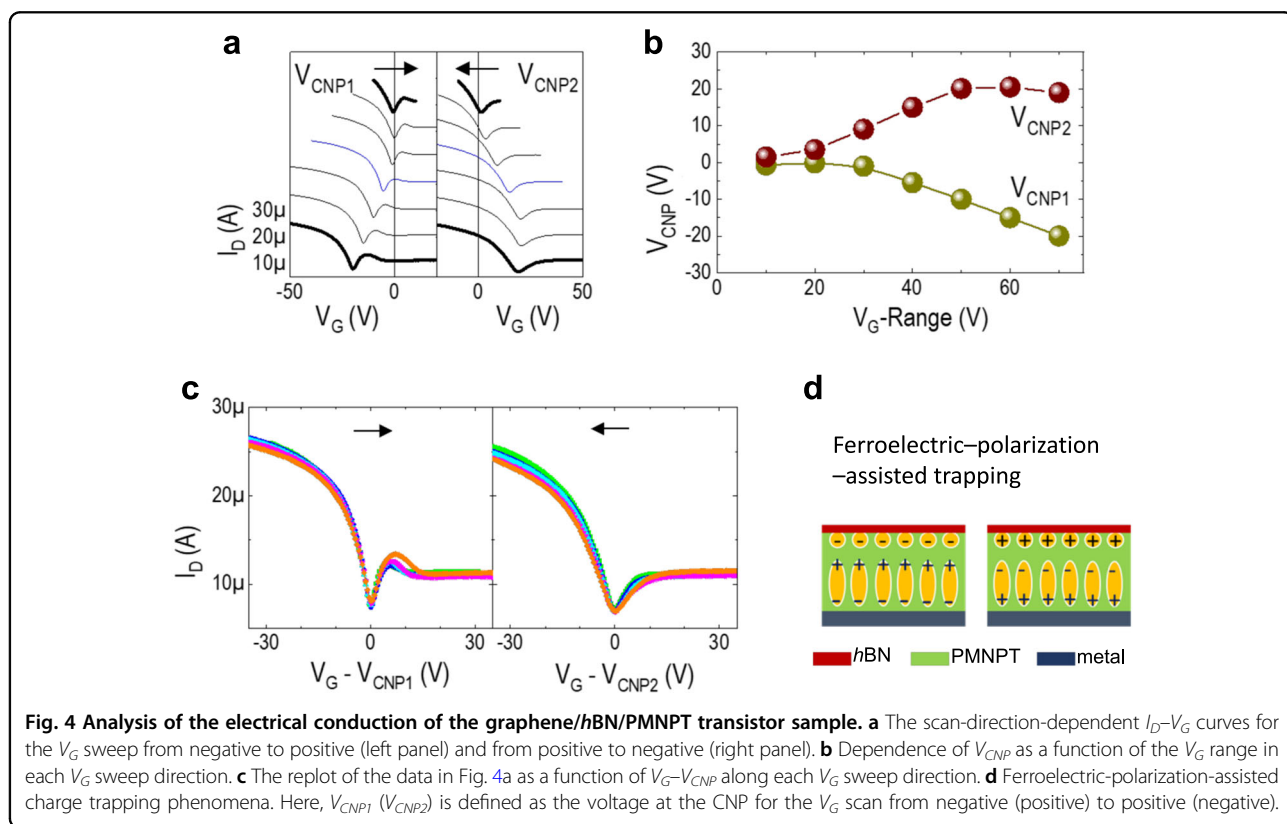
significantly affect the performance of the graphene/PMNPT device. Therefore, the number of trapped holes seems to be proportional to the difference between the coercive voltage and the negative maximum V_G , and trapped charges eventually compensate for the ferroelectric polarization field. Such phenomena can be alternatively interpreted in terms of ferroelectric-polarization-assisted charge trapping, which is to be discussed later.

To help intuitively understand this conductance hysteresis of graphene/PMNPT, we sketch a simplified polarization *versus* electric field (P - E) curve in Fig. 3e and compare it with the real data in Fig. 3f. From the viewpoint of the ferroelectric polarization state, the P - E curve in Fig. 3e can be divided into two parts: one for the polarization-up state and the other for the polarization-down state (which are drawn with the solid, blue-colored line and pink-colored line, respectively). In Fig. 3f, the I_D - V_G curve with a V_G sweep range of ± 60 V is plotted again as an example among many I_D - V_G curves in Fig. 2a, where the data line colors are chosen to match those in Fig. 3e. From a comparison between Fig. 3e, f, for the polarization-up state (i.e., the navy and blue colors half-cycle in Fig. 3e), I_D does not change much while the polarization-up state is maintained, and I_D varies drastically when ferroelectric switching occurs. This result apparently indicates that the ferroelectricity directly affects the graphene charge carrier^{17,18,20–23}. Notably, the majority charge carrier in this

half-cycle is an electron, and it changes to a hole when ferroelectric switching occurs.

On the other hand, the polarization-down state (i.e., the pink and magenta colors half-cycle in Fig. 3e) gives two different I_D values in the negative V_G region depending on the V_G sweep direction, and I_D is almost constant in the V_G region of ferroelectric switching. These behaviors indicate that the graphene's electrical conduction does not seem to be directly coupled with the ferroelectricity of the PMNPT. Therefore, the origin of the overall asymmetric shape in the I_D - V_G curve can be ascribed to carrier-type-dependent interfacial charge trapping at the graphene/PMNPT interface. In other words, the interfacial trap sites are carrier dependent; at these sites, only holes are strongly trapped at the interface because of the negative V_G in combination with ferroelectric polarization²⁸. The detrapping processes of hole carriers occur by performing ferroelectric switching in the opposite direction with no interfacial charge trapping phenomena in the largely positive V_G regions.

In Fig. 4, we depict the detailed analysis for the graphene/hBN/PMNPT system illustrated in Fig. 2b. The positions of V_{CNP1} and V_{CNP2} move in the opposite direction as the V_G sweep range increases, as depicted in Fig. 4a, and their dependencies on the V_G sweep range are plotted in Fig. 4b. It is evident that the hysteresis becomes larger as the V_G scans wider. However, their tendency is different for the V_G sweep ranges wider than ± 50 V,



showing an increasing behavior for V_{CNP1} and saturation for V_{CNP2} . Specifically, when the curves along the same sweep direction are collected as a function of V_G relative to the voltage at CNP, i.e., $V_G - V_{CNP1}$ and $V_G - V_{CNP2}$ in Fig. 4c, they are almost identical irrespective of the V_G sweep range. All the results indicate that the electrical transport of graphene in the graphene/hBN/PMNPT system is not directly affected by ferroelectric switching but indirectly influenced by the ferroelectric-assisted charge trapping phenomena (which is depicted in Fig. 4d), thereby resulting in a shift of the V_{CNP} without any changes in the overall conductance behavior^{24–26,29,30,33,36,37,40}.

Notably, the $I_D - V_G$ curves for both graphene/PMNPT and graphene/hBN/PMNPT samples show a similar I_D saturation in the large positive V_G regions. The most intuitive explanation for such a clear I_D saturation is the effect of saturated ferroelectric polarization^{26,37}. In the case of graphene/PMNPT, direct ferroelectricity-controlled charge carrier modulation can be used to explain the saturating behavior, as depicted in Fig. 3. However, for graphene/hBN/

PMNPT, the ferroelectric-assisted charge trapping model introduced in the abovementioned paragraph in Fig. 4d can be used to explain the result. The model includes the deeper charge trap energy due to the Coulomb interaction of ferroelectric polarization, as depicted in Fig. 4d. Compared with the conventional charge trapping in normal dielectrics^{56–61}, the interfacial charge trapping between the normal dielectric and ferroelectric layers might be considerably stronger. It can also deepen the energy level of shallow trap sites, consequently increasing the number of trap sites^{55,56}. In addition, the screening of ferroelectric polarization switching can hinder the appearance of variations in the $I_D - V_G$ curves during ferroelectric switching. Therefore, the interaction between the trapped charges at the surface of the ferroelectric layer and the ferroelectrically polarized electric dipoles is critical to explain the data observed in Fig. 4.

From Fig. 5, the quality of our device with graphene/hBN/PMNPT can be verified by observing the quantum Hall phenomena. At a low temperature of 2 K, the V_G scan demonstrates a nonhysteretic $I_D - V_G$ behavior at

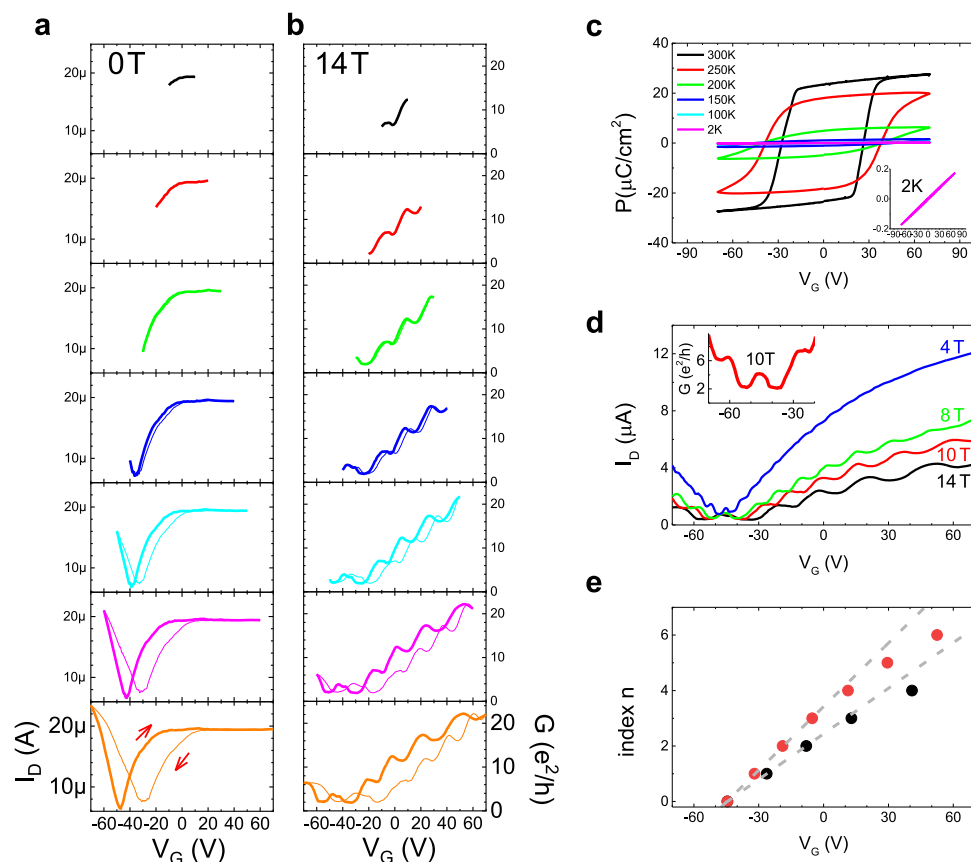


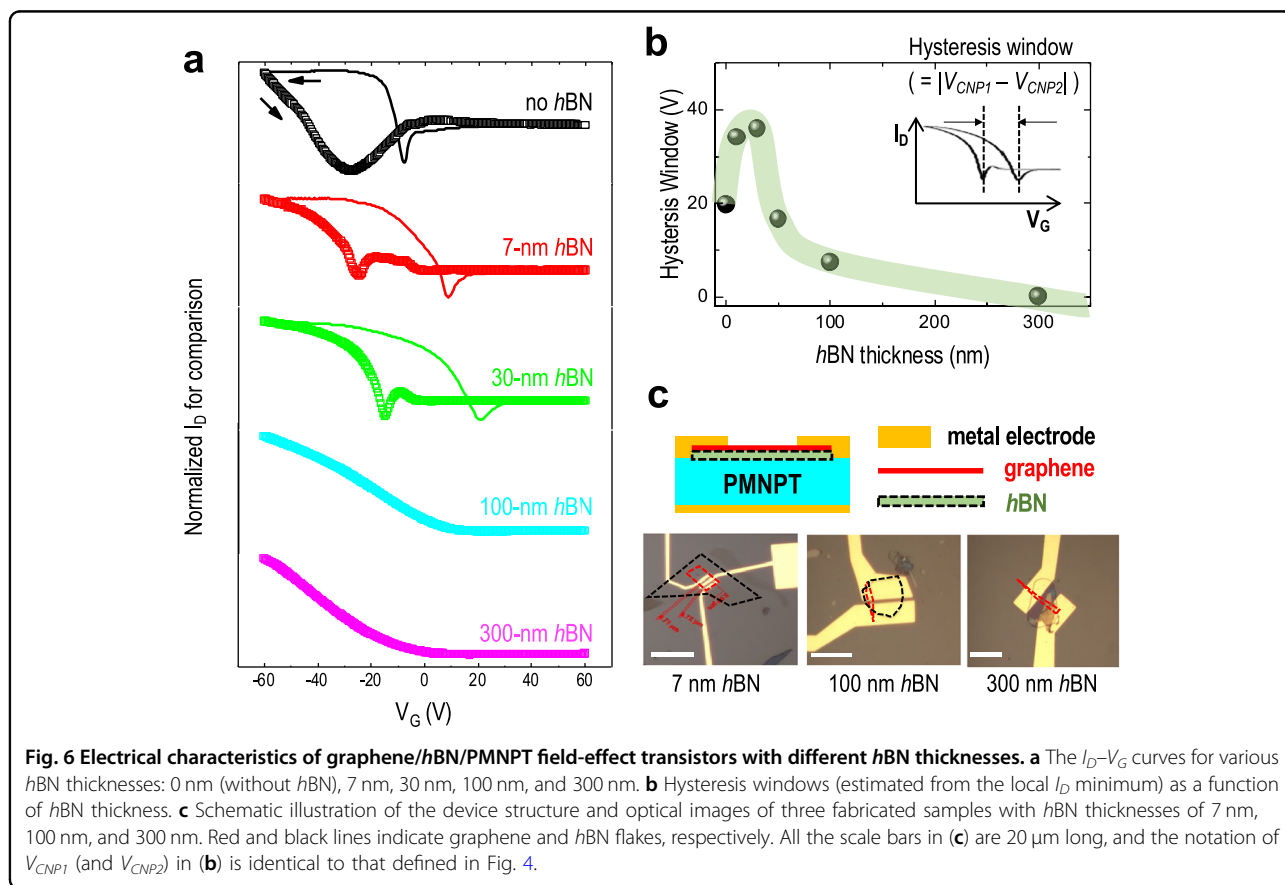
Fig. 5 Observation of the quantum Hall state in the two-terminal graphene/hBN/PMNPT device. **a** The $I_D - V_G$ curves for various V_G sweep ranges at 2 K without a magnetic field. **b** The two-terminal quantum Hall conductance at 2 K and 14 Tesla. **c** The $P - E$ curve as a function of temperature. **d** The $I_D - V_G$ curves at 2 K under various magnetic fields. The inset shows the enlarged quantum Hall conductance data at 10 Tesla. **e** The peak positions of the derivatives of the $I_D - V_G$ curves for 10 (red circles) and 14 Tesla (black circles) in (d), showing a delay in the gate voltage in the development of the next quantum Hall states above 0 V.

narrow V_G sweep ranges, but it becomes hysteretic as the V_G sweep range exceeds approximately ± 40 V, as depicted in Fig. 5a. Such a hysteresis tendency is identical to that in the case in which quantum Hall conductance is observed at 14 Tesla, as depicted in Fig. 5b. Because ferroelectric switching does not occur with frozen polarization at low temperatures, as exhibited in Fig. 5c, the hysteresis in Fig. 5a, b can be attributed to the effect of charge trapping at the interfaces inside the device. From the two-terminal quantum Hall conductance, it is reasonable to assume that charge trapping occurs at the interface between h BN and PMNPT but not at the interface between h BN and graphene⁶¹. In addition, the V_{CNP} at 2 K significantly shifts in the negative V_G region, which corresponds to the intrinsic electron-doping effect of graphene at low temperatures. The origin of this phenomenon can be considered together with the enhanced saturation current in the high V_G region, where the saturation current is approximately 20 μ A at 2 K but approximately 10 μ A at 300 K. This means that the effective electric field applied to the graphene is higher at 2 K than that at 300 K.

In Fig. 5d, we depict the emergence of quantum Hall phenomena in graphene under high magnetic fields, confirming the well-defined states, especially for the filling

factor $\nu = 2$ and 6, as presented in the inset. Only a few previous reports have shown the quantum Hall state of graphene on a ferroelectric substrate^{26,62}. It seems that the 30 nm-thick h BN layer, which functions as an atomically flat thin substrate for graphene⁶³, facilitates the decoupling of the ferroelectric field and graphene. In addition, the trapped charges at the interface between h BN and PMNPT do not hinder the formation of the quantum Hall state because the graphene channel is separate from those traps. On closer examination, the onset V_G of successive quantum Hall states depicted in Fig. 5e becomes delayed as the index becomes higher. This implies that the number of induced charge carriers decreases owing to charge trapping⁶⁴, and it partially contributes to the I_D saturation behavior in the large positive V_G region at a zero magnetic field.

To support the proposed mechanism with more experimental evidence, we collected the results of systematic fabrications and measurements for graphene/ h BN/PMNPT devices while varying h BN thicknesses from 0 nm (i.e., without h BN) to 300 nm, as presented in Fig. 6. The thickness variation in h BN flakes enables the qualitative assessment of ferroelectric-assisted charge trapping by controlling the effect of the ferroelectric substrate on the charge conduction of graphene. In Fig. 6a, we plotted



the I_D – V_G curves of graphene/*h*BN/PMNPT field-effect transistors (with a device structure identical to that in Fig. 1b, f) with *h*BN thicknesses of approximately 0, 7, 30, 100, and 300 nm. Here, the curves of 0- and 30 nm-thick *h*BN samples are the same as those in Fig. 2. For *h*BN flakes 300 nm and 100 nm-thick, the effect of ferroelectricity from the PMNPT substrate was so weak that there was little hysteresis in the I_D – V_G curves. However, in the cases of 30 nm-thick and 7 nm-thick *h*BN flakes, the hysteretic I_D – V_G curves clearly appeared due to the significant effect of ferroelectricity from the PMNPT substrate.

In addition, Fig. 6b shows the hysteresis window defined as the V_G gap between V_{CNP1} and V_{CNP2} (with the same notation in Fig. 4) for each sample in Fig. 6a. Here, the data value for a 50 nm-thick *h*BN sample was estimated from our former work^{29,33}. The general trend is that hysteresis is very weak in thick *h*BN samples but becomes clear and becomes larger in thinner *h*BN samples with anti-hysteresis characteristics. Therefore, we can conclude that the hysteresis occurring in graphene/*h*BN/PMNPT devices is substantially related to the ferroelectricity in PMNPT in combination with interfacial charge trapping between *h*BN and PMNPT, which is interpreted as ferroelectric polarization-assisted charge trapping. However, it is noteworthy that the ‘no *h*BN’ case (*i.e.*, direct contact between graphene and PMNPT, as shown in Fig. 1a) deviates from that trend, which can be ascribed to the results of direct ferroelectric coupling between graphene and PMNPT, at least in the case of electron-majority charge carriers in graphene. Figure 6c is given for a simple side-view illustration of the graphene/*h*BN/PMNPT device under test and the top-view optical images of the fabricated devices having *h*BN thicknesses of 7, 100 and 300 nm. The experimental data of *h*BN’s thicknesses are included in Fig. S5 in SI.

Conclusions

The charge transport of graphene in terms of graphene-ferroelectric interactions is studied using graphene transistor devices with ferroelectric single-crystal PMNPT gate dielectrics. By comparing two device configurations, *i.e.*, graphene/PMNPT and graphene/*h*BN/PMNPT, the direct control of the graphene conductance via ferroelectric polarization switching and the indirect control via polarization-assisted charge trapping at the interface between *h*BN and PMNPT could be identified. The observed quantum Hall conductance in the graphene/*h*BN/PMNPT sample confirms the high device quality and the decoupling of the ferroelectric polarization field from the intrinsic charge conduction of graphene. All these results confirm that charge carriers in graphene can be modulated using the ferroelectricity of the contacting PMNPT substrate. However, such coupling can be hindered because of carrier-dependent interfacial charge

trapping or ferroelectricity-assisted charge trapping phenomena, in which charges are trapped at the interface of the ferroelectric oxide and 2D materials.

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Author contributions

N.P. developed all devices; J.P. and T.K.C. prepared the experimental setups, and N.P., H-Y.K, and D.S. conducted transport measurements. N.P., H-J.K., and D.S. wrote the initial draft, and H.L., H-Y.K, and D.S. analyzed the results in detail and finalized the manuscript. H-Y.K. and D.S. designed and supervised the project.

Competing interests

The authors declare no competing interests.

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