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Next-generation ferroelectric domain-wall memories: principle and architecture

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Abstract

The downscaling of commercial one-transistor–one capacitor ferroelectric memory cells is limited by the available signal window for the use of a charge integration readout technique. However, the erasable conducting charged walls that occur in insulating ferroelectrics can be used to read the bipolar domain states. Both out-of-plane and in-plane cell configurations are compared for the next sub-10-nm integration of ferroelectric domain wall memories with high reliability. It is highlighted that a nonvolatile read strategy of domain information within mesa-like cells under the application of a strong in-plane read field can enable a massive crossbar connection to reduce mobile charge accumulation at the walls and crosstalk currents from neighboring cells. The memory has extended application in analog data processing and neural networks.

Introduction

Ferroelectric memories, which use bipolar domain orientations to store nonvolatile "0" and "1" data, have the advantages of ns-to-ps-scale programming times, almost unlimited cycle endurance, and low-energy consumption.[1,2] The domain size in these memories can be as small as a few nanometers,[3] which is ideal terabit-density storage. Unfortunately, the stored information is read out destructively through a charge integration process using commercial one-transistor–one capacitor (1T1C) or 2T2C architectures, where the signal is reduced with the downscaling of the cell.[1]

Alternative piezoelectric mechanical probes can be used to extract small domain information, but these probes are incompatible with current complementary metal-oxide–semiconductor (CMOS) technology.[4] The channel current can be used to sense the bipolar domain orientations in the gate stack of a ferroelectric field-effect transistor, but this device unfortunately suffers from short retention times (ranging from a few days to months).[5] Another candidate structure for ferroelectric tunnel junction devices has also emerged based on the insertion of an ultrathin ferroelectric film (1–3 nm) between two metal electrodes, in which the quantum-mechanical tunneling current varies with the bipolar domain orientation.[6] However, the integration of monolithic ultrathin films that are free from misfits and defects on large-area silicon wafers in single domain patterns remains challenging. Ferroelectric diode memories, in which the polarity of a unidirectional diode's current can be reversed upon polarization flipping, can use comparatively thicker semiconducting thin films. However, the polarization fatigue and leakage currents become dominant after 10^5 write cycles.[7] These structures are far from the stage of reaching device-level integration.

Out-of-plane domain wall memory

Ferroelectric domain wall memory can function using a "pure ionic" switching mechanism: the charged domain walls that occur in ferroelectric single crystals displayed giant metallic-like conductivity,[8] and the pA-scale currents of the neutral 109° and 180° domain walls in (110) $BiFeO_3$ thin films (indexed as pseudocubic) were observed during piezoresponse force microscopy (PFM) and conductive atomic force microscopy (CAFM) mapping of these films,[9] as shown in Fig. 1a and b, respectively. The

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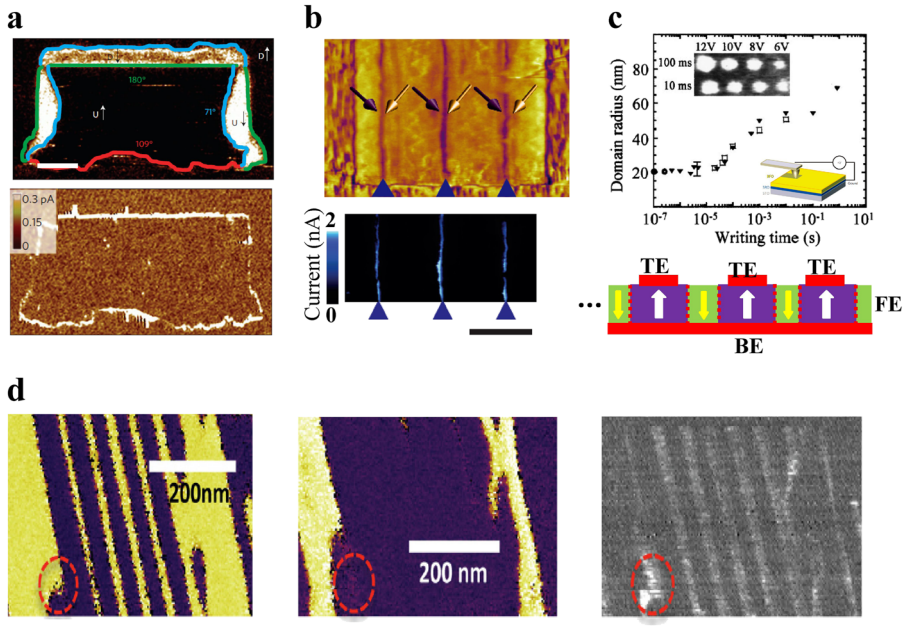

Fig. 1 Out-of-plane wall currents. a and **b** In-plane PFM phase and amplitude images (upper panels) of opposite domain patterns for 100-nm-thick (110) $BiFeO_3/SrRuO_3/SrTiO_3$ thin films with neutral 71° (blue), 109° (red), and 180° (green) walls and for 45-nm-thick (001) $La_{0.1}Bi_{0.9}FeO_3/SrRuO_3/DyScO_3$ thin films with charged 71° walls (scale bars represent 1 μm), where the wall conduction was confirmed by CAFM mapping at −2 and 2.5 V in the lower panels, respectively (adapted from Seidel et al.[9] and Crassous et al.[10] copyrights 2009 and 2015, respectively, Macmillan Publishers Limited). **c** Plot of domain radius as a function of writing time at 12 V acquired by AFM tip scanning of (001) $Pb(Zr_{0.2}Ti_{0.8})O_3/Sr(Nb,Ti)O_3$ thin films (upper panel), where the inset shows two lines of domains that were written with the times and voltages indicated (adapted from Paruch et al. [11] copyright 2001, American Institute of Physics). The lower panel shows the possible wall positions between the top and bottom electrodes (TE and BE) in the cross-sectional view. **d** In-plane PFM phase images of pristine 109° stripe domains (left panel) and erased domains at 1.7 V (middle panel) in a 95-nm-thick (001) $La_{0.1}Bi_{0.9}FeO_3/SrRuO_3/DyScO_3$ thin film. Concomitant CAFM mapping of the same area in the right panel shows conduction traces from previous walls (adapted from Stolichnov et al.[13] copyright 2014, American Institute of Physics)

conducting walls in insulating ferroelectrics can thus be used to read the polarization states.

The weak currents through the neutral walls can be enhanced through the creation of charged walls to accelerate the read speed of the memory. It has been found that the "trailing field" present in the tri-axial control of a scanning PFM probe tip over (001) $La_{0.1}Bi_{0.9}FeO_3$ thin films can create in-plane head-to-head and tail-to-tail polarization components that form ferroelastic charged domain walls, as shown in Fig. 1b (upper panel). The CAFM current map (shown in the lower panel) shows head-to-head wall currents that are as high as ~1.7 nA.[10] Unfortunately, this current decays over time and drops to 0.2 nA after 10 h, which is far from the current required to drive fast-read circuits. Next, the sideways domain motion could lead to a misfit in the wall position outside the top electrode area (causing read failure) in a real memory device (lower panel, Fig. 1c), as confirmed by plots of the growing domain radius as a function of the writing time and the voltage measured using AFM tips with a radius of ~20 nm (as shown in the upper panel).[11] Furthermore, continuous growth of a monodomain over a large-area silicon wafer is challenging, whereas inverted nanodomains generally have poor retention.[12] Finally, long-term persistent domain walls could accumulate opposite mobile charges to compensate for the domain boundary charge that causes the decay in the wall current. Fig. 1d shows an in-plane PFM phase image (left panel) of pristine 109° stripe domains within (001) $La_{0.1}Bi_{0.9}FeO_3$ thin films.[13] The CAFM scans at 1.5 V show no domain wall conduction until the voltage reaches 1.7 V, when domain switching occurs, as confirmed by the in-plane PFM phase image shown in the middle panel; a concomitant current signal appears at the original location of the erased wall, as shown by the CAFM map in the right panel.

The wall currents can be stabilized over a period of several months in rhombohedral BFO nanoislands embedded within a tetragonal BFO thin-film matrix.[14] PFM and CAFM imaging showed that the pristine head-to-head walls formed by quad-domains within each island are center-convergent and insulating, as shown in Fig. 2a. The walls become center-divergent and highly conductive once the tail-to-tail charged walls come into form after poling at +3 V, in contradiction to the highly conductive head-to-head walls observed in Fig. 1b. The confined cross-shaped walls have good contacts with the top and bottom electrodes, which open routes towards the mass manufacturing of out-of-plane domain-wall memory devices.

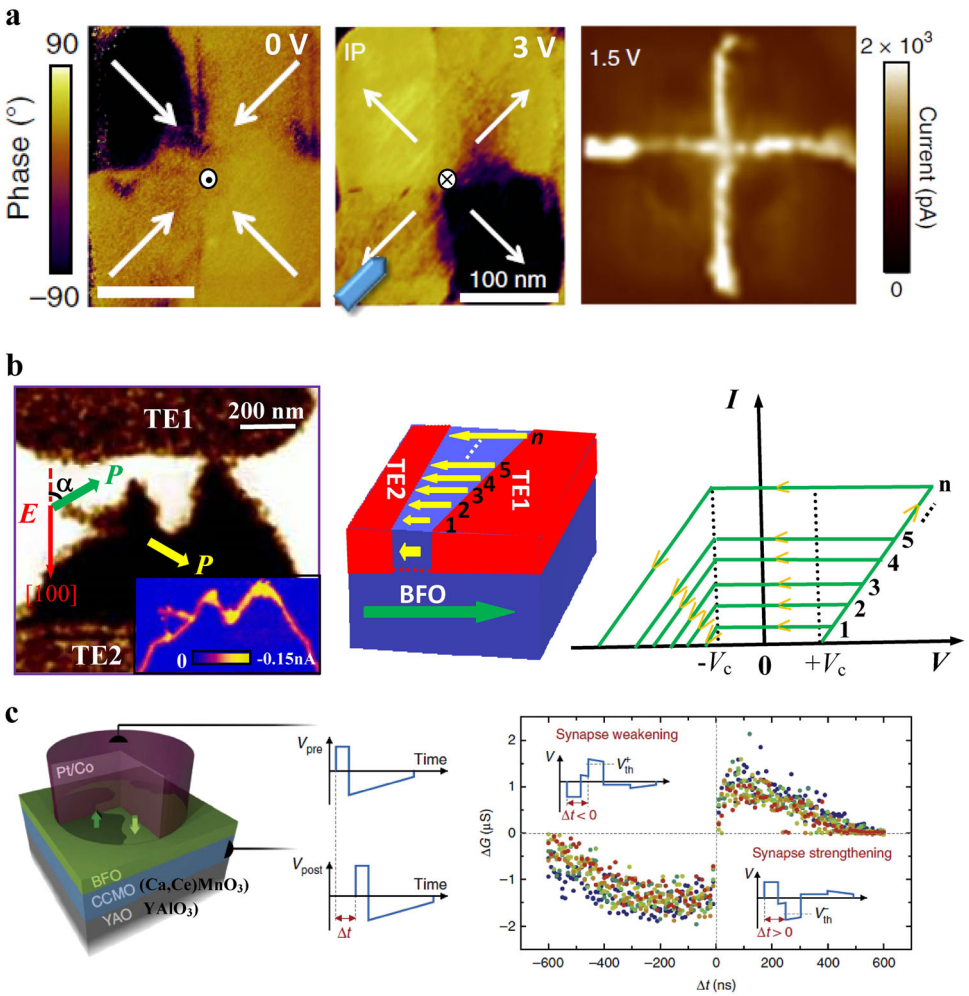

Fig. 2 Artificial synapses and analog data processing. a In-plane PFM phase image of convergent and divergent BFO quad domains after different write voltages (left and right panels) with the appearance of conductive walls envisioned from the CAFM map (right panel) (adapted from Ma et al.[14] copyright 2018, Macmillan Publishers Limited). **b** In-plane PFM phase image of switched polarization ***P*** when it initially intersected with applied electric field ***E*** at an angle *α* with the formation of conductive 71° walls envisioned from the CAFM map in the inset.[16] The middle and right panels sketch the write voltage dependence of the readout wall current proportional to the switched domain number. **c** The conductance of a ferroelectric tunnel junction varies with the delay between pre-synaptic and post-synaptic spikes (adapted from Boyn et al.[18] copyright 2017, Nature Publishing Group)

In-plane domain wall memory

Alternatively, information can be read from the tiny domain via the temporary generation of a high wall current near the film surface under the application of the in-plane read field (***E***) between the two top electrodes (TE1 and TE2).[15,16] Fig. 2b (left panel) shows an in-plane PFM phase image of two switched head-to-head 71° triangular domains in a (001) $BiFeO_3$ thin film,[16] where the in-plane polarization (***P***) intersects with ***E*** at an angle of *α*.[17] The concomitant CAFM image presented in the inset shows the significantly higher electrical conductivity of the entire domain-wall region. The wall current increases nonlinearly with the reduction in the gap length to follow a space-charge-limited conduction process with a thermal activation energy of 0.16 eV;[16] the current increases exponentially with the value of $\sin\alpha$ ($0° \le \alpha \le 90°$), and the wall current is more than 300 nA with $\alpha = 90°$.[17] Once the switching pulse is removed, domain backswitching occurs and erases the walls within a time as short as 16 ns.[16] This temporary domain nature permits the nondestructive reading of nanodomain information while also avoiding long-term defect accumulation at the persistent walls.

The persistent wall current that is proportional to the switched domain number permits multilevel programming of analog data in a triangular geometrically shaped mesa-like cell,[16] as shown in the middle panel of Fig. 2b, where the coercive voltage increases linearly

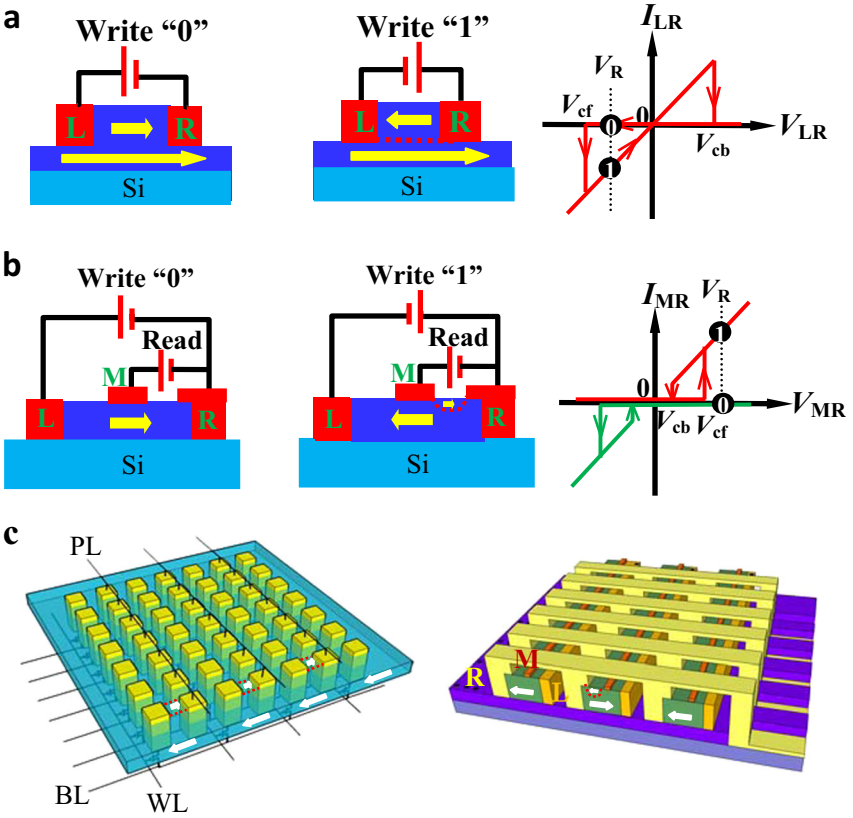

Fig. 3 Working principle and architecture of the in-plane domain wall memory. a and **b** Sketches of two-terminal and three-terminal mesa-like cells with bipolar domain information written at voltages higher than V_{cb} (left panel) and lower than V_{cf} (middle panel) that were applied to the **L** and **R** electrodes, respectively. The right panels show the "off" and "on" current states from the *I*–*V* curves assumed in Ohmic conduction at a read voltage applied between **L** and **R** when $0 > V_R > V_{cf}$ for the two-terminal cells and applied between **M** and **R** with $V_R > V_{cf}$ for the three-terminal cells, accompanied by erasure/creation of the domain walls indicated by dotted red lines. V_{LR}, for example, denotes the voltage that is applied to **L** when **R** is grounded and **M** is floating. The thick arrows indicate domain orientations, and the thin arrows indicate voltage sweeping directions in the *I*–*V* curves. **c** 1T–1R and cross-bar architectures proposed for the two-terminal and three-terminal memory cells, respectively

with the distance between TE1 and TE2. The switched domain number and, thus, the wall current are proportional to the amplitude of a write voltage, as shown in the right panel, which highlights the superiority of the in-plane memory configuration over that of the out-of-plane memory in the storing of multilevel information.

Beyond analog data processing, domain wall memories can also be used in neural networks that require high speed, accurate, and repeatable programming of cells. The conductance based on ferroelectric tunnel junctions can mimic a nanosynapse in neuromorphic architecture that can be finely tuned by voltage pulses and set to evolve according to a biological learning rule called spike-timing-dependent plasticity (STDP),[18] as shown in Fig. 2c. Similarly, STDP can be harnessed from inhomogeneous polarization switching that occurs in both out-of-plane and in-plane domain wall memories.

Read and write architecture

Figure 3a and b show two schemes for the in-plane domain wall memories in cross-sectional views, where each cell is etched into a mesa-like structure with left (**L**), middle (**M**), and right (**R**) electrodes. The **L**/cell/**R** structure forms a parallel-plate capacitor-like structure that provides efficient screening of polarization charge and stabilizes the written ferroelastic domains by eliminating stress-induced instability.[12] If the film has a monodomain structure with a large readout current at a small read voltage (V_R), two-terminal cells etched into the partial film thickness are proposed, as shown in Fig. 3a; here, the written "0" and "1" domains are parallel/antiparallel to the unswitched bulk domain at the bottom (indicated by thick arrows in the horizontal projection) and accompany the erasure/creation of a persistent conductive wall (indicated by the dotted line) under application of a write voltage above the forward coercive voltage of V_{cb} or below the backward coercive voltage of

V_{cf}, respectively. Later, the "off"/"on" currents can be read out when $0 > V_R > V_{cb}$, as shown in the right panel.

For thin films in multi-domain structures, three-terminal mesa-like cells that are etched into the entire film thickness are proposed, as shown in Fig. 3b, where the read field is concentrated between the two ends of **M** and **R** and **R** is partially extended over the cell surface. The outer **L** and **R** permit writing of the bipolar domains, which are both read out at $V_R > V_{cf}$. Because $\boldsymbol{E}$ is antiparallel to $\boldsymbol{P}$, the partial domain switching that occurs near the film surface generates sufficiently high wall currents; after read termination, the switched domain back-switches to its previous orientation, thus avoiding long-term mobile charge accumulation at the wall regions.

In the two-terminal cells, the use of a one-transistor–one resistor (1T–1R) architecture leads to a dense cell occupation per unit area, as shown in Fig. 3c (left panel). Alternatively, a crossbar architecture is proposed for use in three-terminal cells for high reliability (right panel), where the wall elimination that occurs after the read operation can effectively minimize the crosstalk currents from neighboring cells.

During memory-device fabrication, the epitaxial growth of large-area ferroelectric thin films on Si substrates is required using the right buffer layers.[19] Otherwise, the wall currents decay quickly in the polycrystalline thin films due to insulating grain boundaries. Recently, a smart-cut technique has matured that can bond ferroelectric single-crystal thin films to Si circuits at room temperature,[20] which provides a great opportunity to develop the next-generation of domain wall memory.

Conclusions

Various readout techniques for high-density ferroelectric memories are compared; among these methods, the out-of-plane manipulation of conducting charged walls can allow read-out of the bipolar polarization states under a small applied voltage, but the long-term readout current is insufficient (0.2–2 nA) to drive the fast-read circuits required. In contrast, the in-plane manipulation of charged domains that occur on the surface of a memory cell permits the application of a strong read field to provide a significantly enhanced wall current (~300 nA). The domain back-switching (wall erasure) process after read termination can also avoid the accumulation of mobile defects at the walls and the crosstalk currents that occur in massive crossbar connections. Hopefully, ferroelectric single-crystal films bonded to the Si circuits will permit terabit-density integration of the ferroelectric domain wall memory using modern sub-10-nm-node CMOS technologies in the near future.

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Conflict of interest
The authors declare that they have no conflict of interest.

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