

# Pushing the limits

John Warlaumont, vice president of advanced technologies at SEMATECH, a consortium of the world's chip manufacturers, talks to **Nadya Anscombe** about the future of optical lithography.

## ■ What is the current state-of-the-art in optical lithography?

Most companies in the chip industry are now using 193 nm lithography or 193 nm immersion lithography to achieve features as small as 32 or 45 nm half-pitch. Pitch — the size of a line plus a space — represents density in lithography and is a better measure of technical achievement than feature size alone. With clever patterning schemes such as double- or multiple-patterning, half-pitch values of 27 nm can be achieved, which was initially thought impossible using 193 nm lithography. Although 193 nm lithography is still viable today, it is clear that it will be the last truly optical lithography technology. As we approach limits such as the numerical aperture of the lens for immersion lithography, another generation of lithography technology is clearly needed. Feature sizes are not the only driving factor; cost is also a big issue. Double patterning is expensive because it involves performing lithography twice per level and using additional etching steps. This is why many companies are turning to extreme ultraviolet (EUV) lithography. Although not needed until target half-pitch values reach around 22 nm, some companies are choosing EUV lithography for half-pitch values that can be achieved with 193 nm technology simply because EUV is less expensive.

## ■ Is EUV lithography the next-generation method of choice?

Yes. The semiconductor industry has thrown its weight behind this technology and is investing substantial amounts of money to create the required infrastructure. Because EUV lithography is the most difficult and technically challenging lithography technique ever developed, there needs to be an unprecedented level of cooperation within the industry to bring this technology to market by 2012 or 2013 as planned. Lithography is the single most important — and most expensive — piece of infrastructure needed by the semiconductor industry, and companies are now working in earnest to bring EUV lithography to market.

## ■ Why is EUV lithography so difficult?

The main problem is that EUV radiation is absorbed by air and many other materials.



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This means that new optics, new masks and new techniques must be developed to use EUV lithography. It also means that the whole process must take place in a vacuum.

## ■ What technical challenges still need to be overcome before EUV lithography becomes commercially feasible?

There are many technical challenges, but the most important ones relate to the reduction optics, the light source and the masks. An EUV lithography system needs reflective mirrors composed of around 100 layers of material. These layers are often only a few molecules thick and require accuracy at the angstrom level. Furthermore, the light source for EUV is no ordinary laser or light source; it is a plasma generated through either a laser or an electrical discharge method. Although good progress is being made in the development of this light source, the main issue is power. Today's systems deliver only about 10–20% of the required power, but we are confident that the technology will be ready in time. Making defect-free masks for EUV lithography is also a huge challenge and requires a major development investment. Electron beam lithography is currently used to make masks, but its throughput is low. Some companies are trying multicolumn electron beam lithography to increase throughput, but I am not sure this technology will be ready in time.

Extreme ultraviolet lithography can only be brought to market if all the necessary infrastructure is available. Mask technology is one area where investment is lacking, and this needs to be addressed.

## ■ What are the limits of EUV lithography?

We believe EUV lithography can be pushed to produce feature sizes down to 10 nm, so it is a technology that will last for more than one generation of feature size. Every time people make predictions about the limitations of a lithography technique, scientists and engineers find ways to break these barriers. But with EUV lithography, we are starting to reach limits that really are fundamental. For example, we are starting to talk about creating electronic switches made up of only a few atoms. In this case, it is not clear what the limit is and where we will go from there. There will come a time when lithography will no longer drive the electronics industry as it does today. Instead, some other way of making chips will have to be developed.

## ■ What about other lithography technologies?

When it comes to next-generation lithography, there are no viable challengers to EUV lithography for making integrated circuits. However, there are many different types of lithography being developed that could find uses in other applications such as photonic devices, micro-electromechanical systems and memory chips. Nano-imprint lithography is now a commercial reality and Sematech is assessing it for use in the semiconductor industry. Although this technique has great resolution, its use for making integrated circuits is limited because it is a contact form of lithography and therefore introduces too many defects. It has great potential for use in the storage industry, however, where defects are not that critical. Self-assembly is also an interesting technique that could be used to produce finer lines, and this technology has a promising future.

## INTERVIEW BY NADYA ANSCOMBE

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