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Received 11 Oct 2013 | Accepted 28 May 2014 | Published 2 Jul 2014

DOI: 10.1038/ncomms5225

Bottom-up superconducting and Josephson junction devices inside a group-IV semiconductor

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Superconducting circuits are exceptionally flexible, enabling many different devices from sensors to quantum computers. Separately, epitaxial semiconductor devices such as spin qubits in silicon offer more limited device variation but extraordinary quantum properties for a solid-state system. It might be possible to merge the two approaches, making single-crystal superconducting devices out of a semiconductor by utilizing the latest atomistic fabrication techniques. Here we propose superconducting devices made from precision hole-doped regions within a silicon (or germanium) single crystal. We analyse the properties of this superconducting semiconductor and show that practical superconducting wires, Josephson tunnel junctions or weak links, superconducting quantum interference devices (SQUIDs) and qubits are feasible. This work motivates the pursuit of 'bottom-up' superconductivity for improved or fundamentally different technology and physics.

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The Nb/AlO_x/Nb (or Al/AlO_x/Al) Josephson junction (JJ) has become almost ubiquitous for superconducting (SC) applications such as magnetometers¹, voltage standards^{2,3}, logic⁴ and qubits⁵. This follows a long history of development beginning in force with the IBM Josephson digital computer program during the 1970s⁶, which pioneered the tunnelling JJ technology (mostly based on Pb-alloy tunnel junctions, the critical current spread and the instability of the Pb that limited its applicability). Nb-based tunnel junctions such as Nb/Al-AlO_x/Nb (ref. 7) and Nb/AlO_x/Nb (refs 8,9) proved to be more reliable and stable and have become the material of choice in many traditional SC devices, while Al/AlO_x/Al junctions are typically preferred for quantum computing at millikelvin-operating temperatures.

But heterogeneous devices such as these can pose problems, especially for low-power or quantum applications, where losses in or at the interfaces of the various materials (for example, surface oxides on the superconductor, JJ insulator, substrate, interlayer dielectrics) can limit device quality dramatically. Possible solutions include better materials^{10–12}, weak-link junctions¹³, symmetry protection¹⁴ or three-dimensional (3D) cavity qubits¹⁵. Here we consider an alternative approach: atomically precise¹⁶, hole-doped SC silicon¹⁷ (or germanium¹⁸) JJ devices and qubits made entirely out of the same crystal. Like the Si spin qubit, our super-semi¹⁹ JJ devices exist inside the ‘vacuum’^{20,21} of ultra-pure silicon, far away from any dirty interfaces. We predict the possibility of SC wires, JJs and qubits, calculate their critical parameters and find that most known SC qubits should be realizable. This approach may enable better devices and exotic SC circuits as well as a new physical testbed for superconductivity.

Our proposal builds from experimental progress in three different areas. First, the list of SC materials has expanded to include doped covalent semiconductors²², particularly Si (refs 17,23) and Ge (refs 18,24). Extremely high doping rates (of acceptors) above the equilibrium solubility were achieved by gas-immersion laser doping (GILD) or ion implantation and annealing, and SC was observed in these high-density hole systems. Second, rapid progress in precise and high-density doping (of donors) in Si¹⁶ and Ge²⁵ utilizing atomic layer doping and scanning tunnelling microscope (STM) lithography has opened a new world of possible semiconductor devices, including single dopant qubits²⁶, single-atom-wide wires²⁷ and even vertically stacked 3D nanodevices^{28–30}. These same techniques should be applicable to acceptor incorporation. Finally, SC and Si/Ge qubits are widely considered to be leading candidates for fault-tolerant quantum computing; yet both have negatives that combination may improve. For example, coherence times in isotopically enriched and chemically purified Si can reach

seconds²⁰, while SC qubits offer a huge range of design space due to their macroscopic nature. Motivated by these results, we consider the following questions: What are the relevant properties of hole-doped SC ‘wires’ in Si? What is required to create properly placed, hole-doped SC Si JJs? And if such fabrication requirements are plausible, would such devices be of interest for qubits or other JJ circuits? The answers to these questions are not obvious *a priori* given this unusual SC semiconductor system.

Results

Superconductivity in silicon. By doping a semiconductor or an insulator above the metal–insulator transition density, it has been expected that the host material turns into a superconductor¹⁹. Superconductivity has been observed in many such materials. (See refs 22 and 31 for reviews.) Particularly, superconductivity in hole-doped, group-IV materials have been found in diamond³², silicon¹⁷ and germanium¹⁸. Various methods, such as high-pressure high-temperature treatments³² and growth using chemical vapour deposition^{33,34} for C:B, GILD^{17,35,36} for Si:B, and ion implantation and annealing for Si:Ga (refs 23,37) and Ge:Ga (refs 18,24,38), were used to achieve very high hole densities required for superconductivity. Table 1 summarizes the superconducting parameters of the hole-doped group-IV materials including those calculated here. They are compared with the conventional metal superconductors.

Superconductivity in silicon was first reported in ref. 17, by heavily doping a Si layer with boron (B) (above its equilibrium solubility in Si, $6 \times 10^{20} \text{ cm}^{-3}$). This led to the very high hole density of $n_h \approx 5 \times 10^{21} \text{ cm}^{-3}$ and superconductivity was observed below $T_c \approx 0.35 \text{ K}$, although the SC Si layer (thickness $\approx 35 \text{ nm}$) was inhomogeneous with long tails in the superconducting and diamagnetic transitions. Later experiments³⁵ with much more homogeneous samples (thickness $\approx 80\text{--}90 \text{ nm}$) allowed systematic measurements of the dependence of the superconductivity on system parameters, such as the density and the external magnetic field. The highest $T_c \approx 0.6 \text{ K}$ was observed for the B density $c_B \approx 8 \text{ at.}\%$ (1 at.% means 1% of Si atoms are replaced with B atoms, which corresponds to $5 \times 10^{20} \text{ cm}^{-3}$) and the minimum B density c_c for superconductivity was $c_c \approx 2 \text{ at.}\%$. The critical field H_{c2} for $c_B = 8 \text{ at.}\%$ was measured to be 0.1 T. The experimental results agree well with the conventional Bardeen–Cooper–Schrieffer (BCS) theory³⁹ for superconductors of type II.

We estimate the characteristic parameters of this superconductor for $c_B = 8 \text{ at.}\%$. The observed critical temperature $T_c = 0.6 \text{ K}$ corresponds to a zero temperature energy gap

Table 1 | Superconductivity in hole-doped group-IV materials and conventional metals.

Materials	$n_h(\text{cm}^{-3})$	$T_c(\text{K})$	$H_c(\text{T})$	$\xi_0(\text{nm})$	$\xi(\text{nm})$	$\lambda_L(\text{nm})$	$\lambda(\text{nm})$
C:B ³²	4.6×10^{21}	4	3.4	—	10	—	—
C:B ³⁴	8.4×10^{21}	11.4	10.8	—	5.51	—	—
Si:B ³⁵	4×10^{21}	0.6	0.1	1,000	—	60	—
Si:B*	4×10^{21}	0.6	0.1	1,300	57	36	650
Si:Ga ^{23†}	$1 \times 10^{22†}$	7	9.4	—	6	—	3,700
Ge:Ga ¹⁸	4.3×10^{20}	0.45	0.3	—	33	—	$\sim 10^5$
Al ⁴⁰	—	1.18	0.01	1,300–1,600	—	16–50	—
Pb ⁴⁰	—	7.20	0.08	51–96	—	39–63	—
Nb ⁴⁰	—	9.3	0.2	38	—	39	—

Only the parameters observed or estimated in the references cited were shown. All are type II superconductors, except for Al and Pb. For type II superconductors, H_c is upper critical field for doped semiconductors and lower critical field for Nb.

*Estimated values in the main text.

†The superconducting region is at the interface between Si and SiO₂.

‡Peak Ga density.

$\Delta(0) = 1.76k_B T_c = 91 \mu\text{eV}$. The characteristic lengths in an ideal (pure and local) SC and the more realistic effective values from Ginzburg–Landau (GL) theory have the following relations⁴¹:

$$\frac{\xi(T)}{\xi_0} = \frac{\pi H_c(0) \lambda_L(0)}{2\sqrt{3} H_c(T) \lambda(T)} \quad (1)$$

$$\lambda(T) = \lambda_L(T) \left(1 + \frac{\xi_0/l}{J(0, T)} \right)^{1/2} \quad (2)$$

where ξ_0 (ξ) is the BCS (GL) coherence length and λ_L (λ) is the London (effective) penetration depth, respectively. l is the mean free path and $J(R, T)$ is a function of length R and the temperature T defined by BCS³⁹. Using $H_{c2}(0) = \Phi_0/2\pi\xi^2(0)$ with $H_{c2}(0) = 0.1 \text{ T}$ where $\Phi_0 = h/2e$ is the flux quantum, we obtain the GL coherence length $\xi(0) \approx 57 \text{ nm}$. The London penetration depth can be calculated as $\lambda_L(0) = \sqrt{m_h/\mu_0 e^2 n_h} \approx 36 \text{ nm}$ with the hole density $n_h \approx 4 \times 10^{21} \text{ cm}^{-3}$ and the heavy hole effective mass $m_h \approx 0.5m_e$ with m_e being the bare electron mass. Since the system with $l \approx 3 \text{ nm}$ ($\ll \xi, \lambda$) is in the dirty limit, using equations (1) and (2) we obtain $\xi_0 = 12\xi^2(0)/\pi^2 l \approx 1,300 \text{ nm}$ and $\lambda_L(0) (\xi_0/l)^{1/2} \approx 650 \text{ nm}$. The GL parameter $\kappa = \lambda/\xi \approx 11$ is consistent with type II superconductivity. These characteristic lengths are comparable to conventional metallic superconductors.

Superconducting devices in silicon such as JJs, superconducting quantum interference devices (SQUIDs) and SC qubits could be constructed out of hole-doped regions within the crystal. The doping method (GILD) used for demonstrating the highest T_c SC Si crystals so far³⁵ may not be suitable for the epitaxially encapsulated, nanoscale devices envisioned here. Another method provides an alternative route: STM lithography has been used to precisely implant P dopants in Si. STM lithography is a new technique that allows atomically precise doping of semiconductors. We will briefly summarize the steps of P doping in Si. A Si (001) surface with 2×1 reconstruction (dimerization) is prepared and terminated with hydrogen resist. An STM tip is used to selectively remove some of the hydrogen atoms on the surface⁴² (either across broad swaths of the crystal surface or down to single hydrogen atoms), exposing regions of unmasked silicon atoms. A phosphine (PH_3) gas is introduced, which bonds selectively to the exposed silicon sites. At least three adjacent desorbed dimers are needed for a P to replace a surface Si atom. A phosphine molecule is chemisorbed to a dimer, dissociating into $\text{PH}_2 + \text{H}$ at room temperature. Further annealing at 350° allows recombination/dissociation processes, resulting in a P atom incorporated into the top Si layer ejecting a

Si atom¹⁶. In this way, P atoms were then incorporated into the exposed regions (via atomic layer doping), with positioning accuracy to one lattice site⁴³. The resulting 1D or 2D impurity sheet could reach very high doping rate, up to one in every four Si atoms being replaced with a P atom²⁷. It is not necessary to use an STM tip for the hydrogen desorption step, other lithographic techniques may be possible. This process can be repeated to make stacked δ -doped layers as was demonstrated in Ge (refs 28,29) and Si (ref. 30).

Superconducting wires. The SC Si:B realized by GILD was in a 2D layer with a thickness of tens of nanometres. For SC circuits and JJ applications, forming SC wires will be essential. We consider the use of atomic layer doping and STM lithography to dope B (or other acceptor) atoms into the Si crystal to achieve the very high hole density necessary for SC wires. Since this approach achieved a P density much higher than the B density reached in SC Si doped by GILD, higher hole doping rates may be possible (hence possibly higher critical temperatures) together with extremely fine control on the position and size of the SC region. Figure 1a shows a Si crystal doped with acceptor atoms. The lithographic region has length L , width W and depth D . We assume that every k th layer is doped with doping rate of r_D . If N_1 monolayers are doped, the depth $D = (a/4)(N_1 - 1)k$ and the total number of monolayers in the lithographic region are $N_1^{\text{tot}} = (N_1 - 1)k + 1$. The total number of B dopants N_D is given by

$$N_D = \left(\frac{W}{b} + 1 \right) \left(\frac{L}{b} + 1 \right) r_D N_1, \quad (3)$$

where $b = a/\sqrt{2} = 3.84 \text{ \AA}$, with $a = 5.43 \text{ \AA}$ being the lattice constant of Si. To estimate hole density, we have to take into account the finite range of the holes²⁷. For the P impurities with Bohr radius 2.5 nm , the effective electron density region has a diameter d_B ranging from 1 to 2 nm. An isolated B impurity in Si has a Bohr radius of 1.6 nm (ref. 44), and we choose $d_B = 1 \text{ nm}$. Assuming all B dopants are activated, the hole density n_h is given by

$$n_h = \frac{N_D}{(W + d_B)(L + d_B)(D + d_B)}. \quad (4)$$

For W and L much larger than d_B , it is simplified as $n_h = (r_D N_1/b^2)/[(a/4)(N_1 - 1)k + d_B]$. If the B density in a layer could reach the same level as the P in Si ($\sim 25 \text{ at.}\%$), the hole density of a single doped layer is $1.7 \times 10^{21} \text{ cm}^{-3}$, which is above the critical hole density for superconductivity. In this case, using

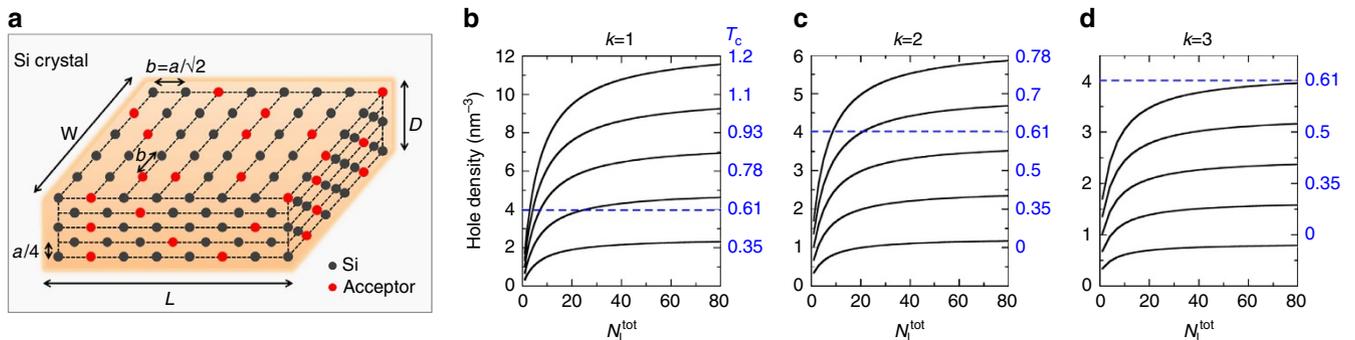


Figure 1 | Hole-doped SC silicon. (a) A specific region inside a single Si crystal, far from any noisy interfaces or surfaces, is hole doped to sufficient acceptor density to go superconducting. The hole cloud, depicted by the orange region, has a larger extent than the lithographically doped region due to finite spread of the hole wavefunction. (b–d) Hole density as a function of the number of total monolayers N_1^{tot} of the doped region for different layer-doping rates $r_D = 5, 10, 15, 20$ and $25 \text{ at.}\%$ from bottom to top. Every layer (b), every other layer (c) and every third layer (d) is doped. The critical temperature T_c is shown on the right side of each plot. The blue dashed line indicates the density $n_h = 4 \times 10^{21} \text{ cm}^{-3}$ corresponding to the highest observed $T_c = 0.6 \text{ K}$ for boron in silicon.

the experimentally observed density dependence of the critical temperature, $T_c = C(c_B/c_c - 1)^{0.5}$ with $C \simeq 0.35$ (ref. 35), we obtain $T_c \sim 0.3$ K, but actual critical temperature could be lower than this due to the thin-layer geometry⁴⁵. The maximum hole density is achieved for a thick doped region ($D \gg d_B$) with every layer being doped ($k=1$). For $r_D = 25$ at.%, $n_h = 1/ab^2 = 1.25 \times 10^{22} \text{ cm}^{-3}$ (a few times more than the highest density obtained by laser doping), we get a maximum $T_c \simeq 1.2$ K, which is comparable to the critical temperature of aluminium (Al). Although this could be possible if all the assumptions here are satisfied, to be more realistic all our calculations below will be for $T_c = 0.6$ K, which has been experimentally realized. Figure 1b–d shows the hole density as a function of depth D when every layer ($k=1$), every other layer ($k=2$) or every third layer ($k=3$) is doped, respectively, for different doping rate r_D . The highest observed T_c of 0.6 K for Si:B should be reasonable for applications, for example, quantum devices based on Al with $T_c \sim 1$ K start to have problems due to quasiparticles at $T \sim 200$ mK, and the requirements for classical applications such as photon detectors are much less restrictive. To reach the $T_c = 0.6$ K, we need at least three doped layers if each layer is maximally doped (25 at.%) for $k=1$, corresponding to the minimum depth of the lithographic layer $D = a/2 = 0.27$ nm and the hole layer $D + d_B = 1.27$ nm. The density strongly depends on the depth for small D (that is, small N_i) and saturates to $4r_D/(kab^2)$ for large D . For thin SC wires, a cross-section area larger than 10^3 nm^2 is preferable (that is, $W, D \gtrsim 30$ nm) to prevent quantum phase slips⁴⁶.

Josephson junctions. JJs are an essential ingredient for many SC applications. Now we describe how one might realize a JJ made of this Si:B superconductor. We will consider two types of JJs: the SC tunnel junction (STJ, Fig. 2a) and the weak-link⁴⁷ JJ (Fig. 2b,c). They are different in the way two superconductors are connected. A STJ consists of two SC electrodes divided by a tunnelling barrier such as an insulating layer, while in weak-link JJs the two SCs are connected by a superconducting or metallic bridge. Traditionally, the STJ has been widely used due to its easier fabrication with a AlO_x barrier and its well-defined nonlinear current–phase relation. Weak-link junctions could be a good alternative especially in applications requiring high Josephson critical current and/or small size junction areas.

Two energy scales that characterize a JJ are the charging energy $E_C = (2e)^2/2C_j$ for junction capacitance C_j and the junction energy $E_j = \hbar I_c/2e$ where I_c is the critical current (maximum d.c. Josephson current). For the capacitance $C_j = \epsilon_r \epsilon_0 A/d$ with $\epsilon_r \simeq 12$ for Si, the charging energy is given by $E_C = 3.0 \text{ eV nm} \times d/A$.

For the STJ, the critical current and the normal resistance R_n has a relation⁴⁸ $I_c R_n = (\pi \Delta)/(2e) \tanh(\Delta/2k_B T)$, which reduces to $I_c R_n = \pi \Delta(0)/2e$ at zero temperature. Here R_n is the resistance of the junction in the normal state. The above relation holds true for the weak link near $T = T_c$, but at $T = 0$, $I_c R_n = 1.32 \pi \Delta(0)/2e$ in the dirty limit⁴⁹. The junction energy at zero temperature then is $E_j = 0.29 \text{ eV} \Omega \times (1/R_n)$ for the STJ and $0.39 \text{ eV} \Omega \times (1/R_n)$ for the weak link.

The normal resistance R_n has a simple form $\rho_n d/A_{wl}$ for a weak link where $\rho_n = 10^3 \Omega \text{ nm}$ (ref. 35). To estimate the normal resistance R_n of the tunnel JJ, we assumed a square potential barrier of width d and height $V_b = E_g/2 + \epsilon_F$ where E_g is the energy gap of Si and ϵ_F is the Fermi energy of the holes for a given density. Then, the tunnelling conductance G per unit area is given by

$$\frac{G}{A} = \frac{m_h e^2}{2\pi^2 \hbar^3} \int_0^{\epsilon_F} d\epsilon_z T(\epsilon_z), \quad (5)$$

where $T(\epsilon_z)$ is the transmission coefficient,

$$T(\epsilon_z) = \frac{4\epsilon_z(V_b - \epsilon_z)}{4\epsilon_z(V_b - \epsilon_z) + V_b^2 \sin^2 \kappa d}, \quad (6)$$

and $\kappa = \sqrt{(V_b - \epsilon_z)2m_h/\hbar^2}$. Tunnelling resistance $R_n = 1/G$. We numerically calculated the tunnelling resistance assuming the hole effective mass $m_h = 0.5m_e$ and obtained $R_n \simeq 10^4 e^{5.6d}/A [\Omega]$ with d in unit of nm and A in unit of nm^2 , for barrier height of $V_b = E_g/2 + \epsilon_F \simeq 2.4 \text{ eV}$ where E_g is the energy gap of Si and ϵ_F is the Fermi energy of holes. Actually, the Fermi energy obtained by using the effective mass at low density is overestimated than the actual Fermi energy of high-density holes⁵⁰, but the barrier height V_b and shape could be significantly modified, for example, by a spatially well-separated heavily doped region acting as a metallic gate. Therefore, the resistance is tunable to a great extent. Figure 3 gives the tunnelling resistance as a function of the barrier width, for different barrier heights. It clearly shows that R_n is proportional to $e^{\alpha d}/A$ for some constant α . By tuning the barrier height, for example, by lowering it, we can significantly relax the requirement on the necessary thinness of the barrier. If $d \lesssim 3$ nm was needed to obtain large enough tunnelling current for $V_b = E_g/2 + \epsilon_F \simeq 2.4 \text{ eV}$, we would need $d \lesssim 7$ nm for $V_b = 1.9 \text{ eV}$.

To overcome thermal fluctuations, the junction energy must be much larger than the temperature. In practice, $E_j \gtrsim 5k_B T \approx 4.3 \mu\text{eV}$ for 10 mK. The barrier distance d of the STJ then must satisfy $d \lesssim 3$ nm for $A = 1 \mu\text{m}^2$. The junction area A cannot be much smaller since then the distance d would need to be very small, but an external gate that could also be built of a separate doped region can control the tunnelling barrier height and shape relaxing the

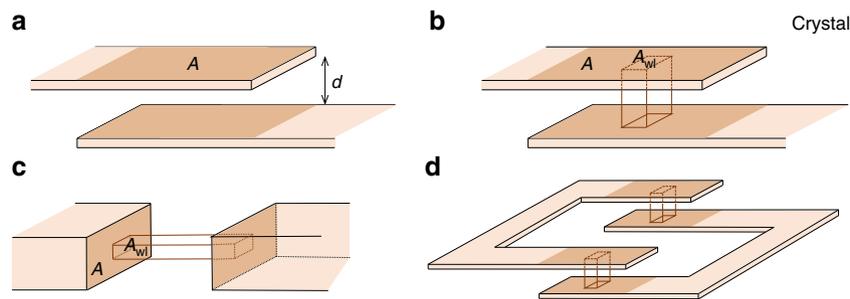


Figure 2 | Super-semi JJs and SQUID geometries. Examples of JJ devices that can be constructed inside the semiconductor are shown. Wire figures depict the extent of the hole wavefunction. **(a)** STJ with overlapping area A separated by distance d . **(b)** Weak-link JJ with overlapping SC layers. Critical current is determined by the bridge of cross-section A_{wl} and length d , while the capacitance is determined by the overlap area A and distance d . This geometry is suitable when a large overlap area A (small charging energy E_C) is required. **(c)** Weak-link JJ in a variable thickness bridge geometry (or STJ with no link), suitable if large A is not necessary. **(d)** SQUID circuit.

restrictions at the cost of more complication in device design. A large junction area would be more easily implemented in the overlapping geometry of Fig. 2a, given that doping a thin layer with large area is probably easier than doping a small but thick region with STM lithography. For the weak link, on the other hand, the required condition is $A_{w1}/d \gtrsim 0.01$ nm, which could be easily satisfied, and the junction energy is independent of the total junction area A . Hence, both Fig. 2b,c would be possible.

If we want to avoid hysteresis in the I - V curve as is usually required for dc SQUID application, we need an overdamped JJ and the junction quality factor $Q = \omega_p RC_J$ must be smaller than 1, where $\omega_p = \sqrt{2E_C E_J}/\hbar$ is the plasma frequency of the JJ. R is of the order of R_n for the weak link and $R \sim R_n e^{A/k_B T}$ for the STJ. For the STJ to satisfy $Q < 1$, typically a shunting resistance would be necessary to reduce the total resistance, since R is very large for an isolated tunnel junction (one would want to avoid this for quantum applications). Alternatively, SC-Insulator-Normal metal-Insulator-SC (SINIS)-type junctions⁵¹ may be advantageous for achieving an overdamped JJ. For the weak link, $Q = 5.5 \times 10^{-3} \sqrt{A/A_{w1}}$ and for $A_{w1} = 100$ nm², $A < 3.3$ μ m², allowing much smaller size than the STJ.

For a SQUID application such as shown in Fig. 2d, additional conditions should be satisfied to avoid magnetic hysteresis: $\beta_m = 2LI_c/\Phi_0 < 1$ where L is the inductance of the SQUID loop. STJs can easily satisfy this since the critical current is small, but a fairly large loop would be needed due to the large junction area $A \approx 1$ μ m² required to overcome the thermal fluctuations as discussed above. On the other hand, weak-link JJs open up the possibility of a nanoscale SQUID. For a square loop of area 1 μ m \times 1 μ m, the geometrical inductance L is ~ 3 pH for wire diameter of a few tens of nm, assuming that the relative permeability of doped Si is one like most nonmagnetic metals. Then, $\beta_m < 1$ translates into $A_{w1}/d < 2 \times 10^3$ nm. Typical values $A_{w1} \approx 100$ nm² and $d \approx 10$ nm would be suitable for a nano-SQUID. Compared with the nano-SQUID based on the metallic SC bridges⁵², we could get much shorter weak links due to the much higher precision of STM lithography over electron-beam lithography, allowing one to reach the short link limit with highly nonlinear inductance and larger modulation depth in critical current.

Qubits. Finally, we consider the possibility of SC qubits in Si:B. The requirements on JJ parameters for qubits are different from the conditions, for example, SQUID discussed in the previous section. We will consider the core SC qubits—charge, phase and flux—to estimate relevant parameters, noting that more complicated designs would relax the restrictions on the parameters significantly. A charge qubit is a single Cooper pair box connected to a JJ where the two discrete low-energy levels form a logical qubit space. Usually, a gate voltage is applied to tune the system to be in a sweet spot to reduce the effects of the charge noise, but in this case its known sensitivity to charge noise might make a good probe of the charge environment of this system. Figure 4a shows a possible geometry for a charge qubit and Fig. 4b is the equivalent circuit diagram. By choosing different geometries for the two tunnel junctions, for example, $d_1 \lesssim 3$ nm and $d \gtrsim 10$ nm, the left junction can have large enough JJ energy to act as a JJ, while the right junction has negligible JJ energy and can be considered as a simple capacitor with capacitance C_g . The charge qubit is operated in a regime $k_B T \ll E_J \sim E_C \ll \Delta$ where E_C is now the total charging energy $E_C = (2e)^2/2(C_1 + C_g)$. Assuming $T = 10$ mK, a JJ with $d_1 = 2.5$ nm means that A_1 should be ≈ 1 μ m². The charging energy $E_C = 3.0$ eV nm $\times 1/(A_1/d_1 + A/d)$ with $d_1 = 2.5$ nm and $A_1 = 1$ μ m² constrains the geometry of the capacitor $A/d \ll 3.1 \times 10^6$ nm. So we can choose, for example, $A \sim 10^6$ nm² and $d \sim 20$ nm.

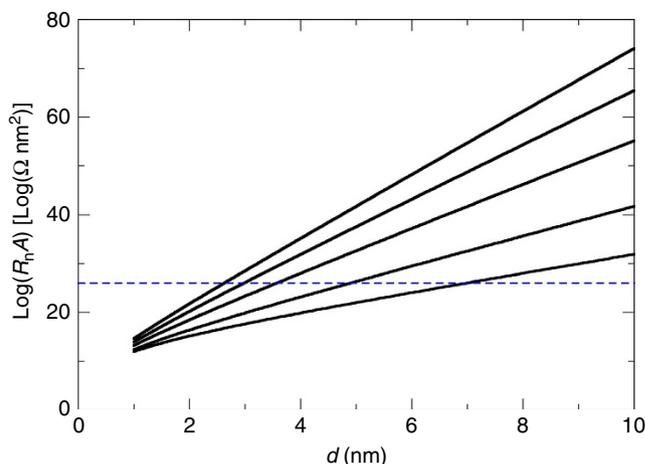


Figure 3 | Tunnelling resistance R_n as a function of barrier width d . Hole density is $n_h = 4 \times 10^{21}$ cm⁻³, and the barrier heights V_b are, from top to bottom, $V_b = 2.6, 2.4, 2.2, 2.0$ and 1.9 eV. The dotted blue line indicates a tunnelling resistance corresponding to $V_b = 2.4$ eV and $d = 3$ nm.

High JJ critical current makes the phase qubit a good choice for the weak-link JJ. Figure 4c shows a circuit diagram for a simple phase qubit. A phase qubit operates in a regime with $k_B T \ll E_C \ll E_J$, which translates into $d/A \gg 3 \times 10^{-7}$ nm⁻¹ and $AA_{w1}/d^2 \gg 7.7 \times 10^3$ nm². A reasonable set of parameters would be, for example, $d \sim 10$ nm, $A_{w1} \sim 100$ nm² and $A \sim 10^6$ nm². For the flux qubit, the simplest model is a loop with a JJ (radio frequency (rf)-SQUID loop) coupled to an externally supplied flux. The flux qubit operates usually with $L_J \lesssim L$, where $L_J = \Phi_0/2\pi I_c$. The loop inductance is relatively quite small compared with L_J for the typical geometries we have considered so far. This restriction can be lifted by using, for example, a three JJ loop^{53,54}. More advanced qubits such as the transmon qubit⁵⁵ are realizable by incorporating a big capacitor in the system, which is straight forward. In that case, the JJ can have a small junction area A and both geometries in Fig. 2b,c could be used.

Discussion

Our proposal is promising for new types of JJ devices. The noise environment of buried dopant layers has been reported to be quite low⁵⁶, which is motivating for quantum applications, but obviously not sufficient. Fabrication requirements, as envisioned, have already been realized in the Si:P or Ge:P systems. Many JJ device and qubit geometries are possible beyond what are considered here, which may further reduce fabrication needs; lattice-site precision of impurities is not a fundamental requirement. An assumption in this work is the plausibility of acceptor placement with atomic layer doping and STM lithography. B is currently being pursued in this context, but it is unproven whether the chemistry of adsorption and incorporation (for example, of B₂H₆) will work in a similar manner as PH₃, nor whether the same densities can be achieved (one in four atoms per ML). We have accounted for this by considering lower densities per monolayer. Quick B diffusion and clumping may limit further thermal anneal budgets, but this problem has already been overcome with low-temperature molecular beam epitaxy (MBE)⁵⁷. Local strain due to the strong B bonds is almost certainly present, but does not effect the epitaxial nature of the crystal¹⁷. As potentially better dopant alternatives, Al (AlH₃) or Ga (GaH₃) for both Si and Ge should be pursued, as well as more advanced chemistry and surface preparation approaches for STM lithography and doping

(for example, BCl_3 is used in GILD, so Cl might be considered instead of H).

The extension of the hole cloud (~ 1 nm) would limit the sharpness of the SC region and hole density would drop to zero over this length. Since it is much smaller than the SC coherence length, the entire hole cloud is expected to be superconducting due to the proximity effect. One of the advantages of this single-crystal device could be that there would be no Schottky barrier between heavily doped (metallic) region and lightly doped (semiconducting) region, and no interface states are expected in the interface between doped and undoped regions.

Stacked multilayer designs of electron-doped Si devices were already demonstrated experimentally³⁰. A second doped layer was grown on top of a nanowire capped by undoped Si of 50–120 nm thickness. The whole device was grown epitaxially. The rather large separation between two doped layers in the experiment was needed to obtain smoother surface for the STM lithography of the top layer and also to get enough separation so that the top layer works as a metallic gate. On the contrary, we need the hole wavefunctions to overlap between layers for the 3D SC region. Thus, we need much smaller separation between layers, and this could be a challenge. In fact, Ge may offer significant benefits over Si for JJ devices. Ge's clean surfaces and lower thermal requirements for good epitaxial growth^{28,29} may allow for more and better 3D doped layers as compared with Si (where the limits of epitaxial growth are more likely to result in surface roughness), with less diffusion due to thermal activation anneals.

It is unclear what critical temperatures are possible in pure Ge (or Si) with other acceptors (critical temperatures of up to 7 K (ref. 23) have been reported in Si:Ga/SiO₂ interface structures and even higher for diamond, and numerical simulation⁴⁹ suggests that Al can lead to a higher critical temperature than B in Si). We have focused on Si due to the greater amount of experimental data versus density to guide our device proposals. Theory does not preclude electron-doped SC semiconductors^{19,49}, but experimental efforts have so far shown no evidence⁴⁴.

The AlO_x -based tunnelling JJ has been very successful in many applications over the years, and other materials and different structures have also been studied for various devices⁵⁸. Building SC devices inside a semiconductor proposed here gives several advantages over conventional approaches. The availability of ultra-pure ²⁸Si with < 50 p.p.m. ²⁹Si (ref. 59) and the atomically precise positioning of dopants by STM lithography can help suppress the subgap states due to impurities in the JJ, which is one of the main decoherence channels of SC qubits. Flux noise is another possible source of decoherence for the SQUID⁶⁰, phase qubit^{61,62} and flux qubit^{63,64}. It was suggested that the flux noise comes from the fluctuating spins at interfaces and surfaces of the device^{65,66}. Hyperfine interaction was proposed as a possible mechanism for the relaxation of the surface spins⁶⁷. The lack of nuclear spin in enriched Si at the surface, the separation of the active device region from the surface and the single-crystal structure of the whole device should help significantly reduce the flux noise. The epitaxially grown barrier in this proposal should also reduce any potential two-level fluctuators, as was shown for a crystalline Al_2O_3 barrier^{68–70}. In the Al/ Al_2O_3 /Al junctions, the critical current density showed a wider variation than amorphous AlO_x barriers. A qubit can be designed to be tolerable to these variations in junction critical current, but it involves a more complicated structure⁷¹. For precisely positioned Si:B/Si/Si:B junctions, we expect less variations in system parameters for identically designed devices; barrier quality would be less important for weak-link JJs. Further, the devices can be constructed well below the surface of the semiconductor, away from oxide interfaces that typically cause

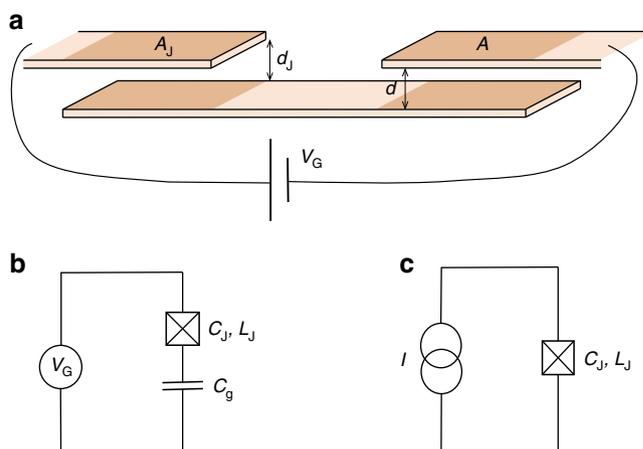


Figure 4 | Superconducting qubit circuits. (a) Example, charge qubit made of tunnel junctions. One tunnelling junction (A_J, d_J) acts as the JJ and the other (A, d) acts as just a capacitor by choosing different parameters. (b) Equivalent circuit diagram of a. (c) Circuit diagram for phase qubit (current-biased JJ), suitable for weak-link JJ.

loss. The quality of the superconducting semiconductor itself is a new concern, and a good early experiment would be to determine the loss of such a device (for example, via a cavity Q). Intriguing in these systems is the possibility of dissipation/quasiparticle engineering by manipulating the disorder of the implanted impurities.

Since the SC properties depend on the hole density, material parameters can be tuned with additional gates, allowing for a tunable SC-normal metal-SC JJ⁷². In that case, the proximity effect will play an important role and needs to be fully taken into account, a topic also of interest in Majorana physics. In addition to these potentially improved material properties, STM lithography is suitable for small devices such as the nano-SQUID and allows for arbitrary 3D device designs for different types of qubits, detectors, circuits and so on.

Progress in 'bottom-up' fabrication techniques, such as STM lithography, has increased the space of devices worth pursuing. Our work further motivates the investigation of acceptor doping via precision techniques, beyond the context of single acceptor qubits⁷³ or for nanoscale but classical electronic devices. Successful demonstration of such proposed physics could not only enable the devices suggested in this work, but also offer an atomically configurable testbed for the nature and limits of semiconductor superconductivity (through, for example, isotope variation, density, disorder, phonon, strain and so on), for T_c engineering, as well as for new devices such as 3D SC device geometries, top-gated tunable JJs or topological qubits⁷⁴.

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Acknowledgements

We thank R. Butera, M. Friesen, A. Mizel, B. Palmer and R. Ruskov for critical reading of the manuscript, and R. Joynt for useful conversations.

Author contributions

C.T. planned the project. Y.-P.S. performed the theoretical and numerical calculations. Both the authors contributed to the interpretation of the results, discussions and writing of the manuscript.

Additional information

Competing financial interests: The authors declare no competing financial interests.

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How to cite this article: Shim, Y.-P. and Tahan, C. Bottom-up superconducting and Josephson junction devices inside a group-IV semiconductor. *Nat. Commun.* 5:4225 doi: 10.1038/ncomms5225 (2014).