

## ARTICLE

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# Resonant tunnelling and negative differential conductance in graphene transistors

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The chemical stability of graphene and other free-standing two-dimensional crystals means that they can be stacked in different combinations to produce a new class of functional materials, designed for specific device applications. Here we report resonant tunnelling of Dirac fermions through a boron nitride barrier, a few atomic layers thick, sandwiched between two graphene electrodes. The resonance occurs when the electronic spectra of the two electrodes are aligned. The resulting negative differential conductance in the device characteristics persists up to room temperature and is gate voltage-tuneable due to graphene's unique Dirac-like spectrum. Although conventional resonant tunnelling devices comprising a quantum well sandwiched between two tunnel barriers are tens of nanometres thick, the tunnelling carriers in our devices cross only a few atomic layers, offering the prospect of ultra-fast transit times. This feature, combined with the multi-valued form of the device characteristics, has potential for applications in high-frequency and logic devices.

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**M**ultilayer stacks of graphene and other stable, atomically thin, two-dimensional materials such as boron nitride, the metallic dichalcogenides and layered oxides<sup>1</sup> offer the prospect of creating a new class of heterostructure materials. Devices based on these materials have been investigated in a number of recent experimental and theoretical papers<sup>2–28</sup>. By fine-tuning the composition of the stacks, it may be possible to create materials with novel electronic and optical properties, which outperform conventional semiconductors. In this article, we use this technology to fabricate and study a resonant tunnelling device in which carriers tunnel through a thin boron nitride barrier layer sandwiched between two graphene electrodes across which a bias voltage is applied. We mount the layers on the oxidized surface of a doped silicon substrate, which we use as a gate electrode. The additional tuning provided by the gate electrode allows us to probe in detail the physics of resonant tunnelling of Dirac fermions and to exploit graphene's unique electronic spectrum, whereby the carrier type (electron or hole) and sheet density can be controlled by the electrostatic field effect<sup>12,23</sup>.

Here, we observe a strong resonant peak in the current-voltage characteristics of the device over a wide range of gate voltages with peak-to-valley ratios (PVRs) of up to 4-to-1. The peak and resulting negative differential conductance (NDC) persist up to room temperature. A model for the carrier tunnelling based on a transfer Hamiltonian approach provides a good fit to the measured device characteristics.

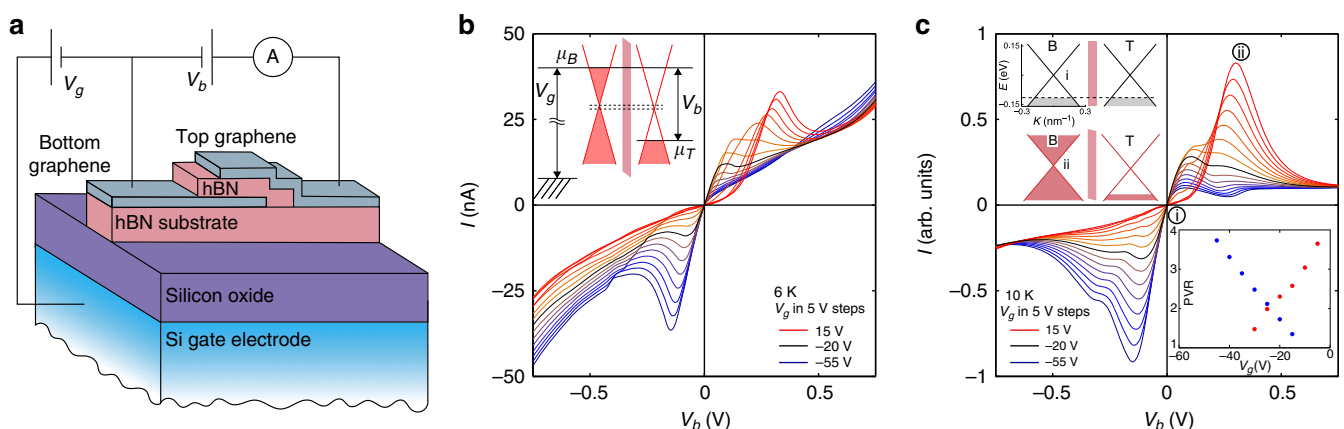
## Results

**Device structure.** The structure of our devices is shown schematically in Fig. 1a. A thick layer of hBN is placed on top of an oxidized Si substrate and acts as an atomically-flat substrate<sup>2</sup> on which the active part of the device is mounted. This consists of two graphene electrodes on either side of an atomically thin hBN tunnel barrier. A tunnel current is generated when we apply a bias voltage,  $V_b$ , between the bottom and top graphene electrodes; the

gate voltage,  $V_g$ , is applied between the doped silicon substrate and bottom electrode. This arrangement allows us to align the Dirac points of the two graphene electrodes while maintaining control of their chemical potentials, as shown schematically in the inset of Fig. 1b. Owing to the low density of states close to the Dirac point, the bottom graphene electrode only partially screens the charge that is induced on the Si-gate electrode by  $V_g$ ; hence the sheet carrier density in the top electrode is also influenced by  $V_g$ . This behaviour is related to the so-called quantum capacitance<sup>29</sup>, which is a strong effect in graphene, unlike the case of conventional semiconductors. A relatively modest  $V_g$  is sufficient to induce a large change in the chemical potential,  $\mu_B$ , of the bottom graphene layer, thus providing additional control of the effective barrier height and transmission coefficient<sup>12,23</sup>.

**Low-temperature measurements.** The main body of Fig. 1b shows the measured gate-dependent resonant tunnelling characteristics for one of our devices, device A, in which the hBN barrier is four atomic layers thick. Unless stated otherwise, the following discussion of the physics and modelling is focussed on measured characteristics of this device. The most notable feature of the data is the presence of a pronounced peak in the current, whose amplitude and voltage position are sensitive to  $V_g$ . Beyond the peak, there is an extended region of NDC. This high-bias regime was not explored in earlier work on graphene-based tunnelling transistors<sup>12</sup>. The  $I(V_b)$  curve is approximately symmetric at  $V_g \approx -20$  V (black curve), but becomes increasingly asymmetric as  $V_g$  is tuned away from this voltage. Although the PVR is relatively small for the symmetric  $I(V_b)$  curve, it is significantly enhanced by tuning  $V_g$ , reaching a value of  $\approx 2$  at  $V_g = -55$  V. Note also that the  $V_g$ -induced increase in the peak height and PVR for one polarity of  $V_b$  is accompanied by a corresponding decrease for the opposite polarity.

**Theoretical model.** To make a direct comparison with the experimental data, Fig. 1c shows theoretical simulations based on



**Figure 1 | Graphene-BN resonant tunnelling transistor.** (a) Schematic diagram of the devices. (b) Measured current-voltage characteristics of one of our devices (device A) at 6 K. The hBN barrier is four atomic layers thick, as determined by atomic force microscopy and optical contrast<sup>13</sup>; the active area for the flow of tunnel current is  $0.3 \mu\text{m}^2$ . The  $V_g$  values range, in 5 V steps, from +15 V (top red curve), through -20 V (black symmetric curve) to -55 V (bottom blue curve). The inset shows schematically the relative positions of the Fermi energies (chemical potentials) of the doped Si substrate gate electrode (represented by hatched lines) and of the two graphene layers at the peak of the  $I(V_b)$  curve in forward bias with  $V_g = +15$  V. (c) Theoretical simulation of device A obtained by using the Bardeen model and including the effect of doping in both graphene electrodes. Parameters:  $q_c^{-1} = 12$  nm; bottom layer is  $n$ -doped at  $4.4 \times 10^{11} \text{ cm}^{-2}$  and the top graphene  $p$ -doped at  $1.0 \times 10^{12} \text{ cm}^{-2}$ . As our top graphene layers are exposed to the environment, we expect them to have stronger residual ( $\sim 10^{12} \text{ cm}^{-2}$ ) doping than the bottom layers, as often observed in partially encapsulated double-layer graphene devices<sup>5</sup>. The top inset (i) shows the chemical potentials  $\mu_T$  and  $\mu_B$  in the top (T) and bottom (B) electrodes, respectively, for  $V_b = 0$  and  $V_g = -20$  V, which corresponds to the symmetric  $I(V_b)$  shown in black; for inset (ii)  $V_g = +15$  V and  $V_b = 0.3$  V, which corresponds to the peak of the  $I(V_b)$  curve. The lower inset shows the  $V_g$  dependence of the  $\text{PVR} = I_p/I_v$  obtained from our simulations, where  $I_p, I_v$  are the currents at the peak and the valley (minimum) beyond.

the Bardeen transfer Hamiltonian approach, which includes the effects of residual doping in the graphene electrodes on the device characteristics. Before discussing this figure in detail, let us first consider an idealized case in which the graphene electrodes are undoped and their crystal lattices are aligned. If  $V_g = V_b = 0$ , the Fermi energy,  $\mu$ , in each layer is at the Dirac point and the two Dirac points are at the same energy, as shown in inset (a) of Fig. 2. If  $V_b > 0$ , electrons accumulate in the negatively biased electrode with an equal number of holes in the positive electrode (inset (b) of Fig. 2). This charging of the two layers generates an electric field, which misaligns the two Dirac points. Therefore, in order for a carrier to tunnel from one electrode to the other, its in-plane wavevector  $\mathbf{k}$  must change. Such a change is forbidden unless the tunnelling event is accompanied by a scattering process in which the conservation of  $\mathbf{k}$  is relaxed. Figure 2, inset (c), shows the effect of a positive  $V_g$  on the Fermi energies in the two graphene electrodes when  $V_b = 0$  so that the two chemical potentials are aligned. Keeping  $V_g$  fixed, we can adjust  $V_b$  to bring the Dirac points of the two electrodes into alignment, see Fig. 2 inset (d), thus allowing all carriers whose energies are between the now distinct chemical potentials of the two electrodes to tunnel resonantly.

In real devices, elastic scattering due to disorder or interaction effects leads to relaxation of the  $\mathbf{k}$  conservation condition, so that the resonant feature which appears in the current-voltage curves has a line-width and position that depend on the disorder potential or the nature of the interaction. This type of behaviour has been investigated in conventional III-V heterostructure devices in which carriers tunnel resonantly through a barrier sandwiched between two confining quantum wells, so-called '2D-to-2D tunnelling'<sup>30,31</sup>.

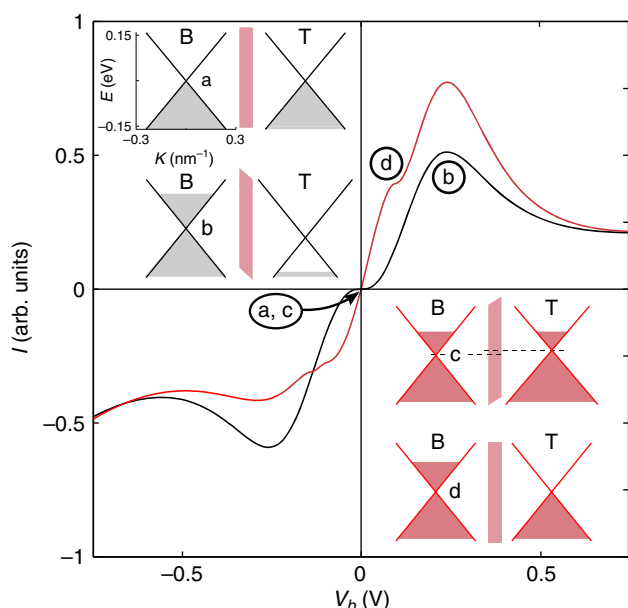
For a tunnelling electron, a disorder-induced change,  $q$ , in its in-plane wavevector can be described in terms of a scattering potential,  $V_S(q)$ . If  $V_S(q)$  is weakly dependent on  $q$ , the tunnel current increases monotonically with  $V_b$ , so no peak is observed. However, a resonance can appear if  $V_S(q)$  has a bell-shaped

dependence, falling towards zero when the magnitude of  $q$  exceeds a certain value  $q_c$ , where  $q_c^{-1}$  is the lower limit of the modulation length of the disorder-induced scattering potential in real space. To model our data, we use a short-range scattering potential,  $V_S(q) \propto 1/(q_c^2 + q^2)$ , where  $q_c^{-1} = 12$  nm. Such a  $V_S(q)$  can arise from potential variations associated with electron-hole puddles<sup>32</sup>, short-range disorder<sup>33,34</sup>, the Moiré pattern at graphene-hBN interfaces<sup>10,35,36</sup> (there are three such interfaces in our device) and/or acoustic phonon scattering. The simulations shown in Fig. 2 are qualitatively similar to those observed for our devices. The region of NDC corresponds approximately to  $V_b \sim \hbar v_F q_c / e$ , the situation where the typical in-plane wavevector change,  $q$ , approaches  $q_c$ ;  $v_F$  is the Fermi velocity in graphene.

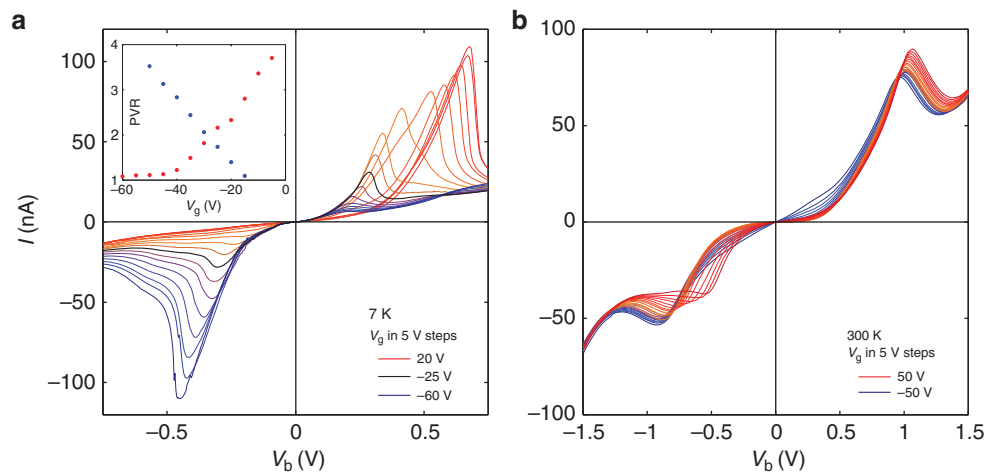
**Theoretical model of the measured device characteristics.** We now focus on the quantitative features in the measured  $I(V_b)$  curves, which are not reproduced in the simulations using undoped graphene layers. Note, first, that the measured differential conductance at  $V_b = 0$  is finite at all values of  $V_g$ , see Fig. 1b, whereas in Fig. 2 it tends to zero at  $V_b = 0$  for the (black) curve with  $V_g = 0$ . Second, the measured  $I(V_b)$  curves are symmetric at  $V_g = -20$  V, whereas for the model calculation in Fig. 2 the curve is symmetric at  $V_g = 0$ . Our model successfully reproduces these features when we take into account the effect of unintentional, residual doping of the graphene layers. As can be seen by comparing Fig. 1b and c, good quantitative agreement between experiment and theory for device A is obtained when the residual doping has the values stated in the figure caption. All the essential features of the measured  $I(V_b)$  characteristics are then reproduced: the  $V_g$  dependence of the linear conductance around zero bias due to the finite density of states—see inset (i) in Fig. 1c; the  $V_g$ -induced shift of the peak in current and the NDC region beyond; the way in which the application of  $V_g$  enhances the peak in  $I(V_b)$  and associated NDC in one bias direction, while decreasing it in the other bias direction.

The strong peak in  $I(V_b)$  arises from the resonant alignment of the energies of Dirac cones in the two electrodes and the large number of empty states in the top electrode, which are available to electrons tunnelling from the bottom emitter layer, as illustrated in inset (ii) of Fig. 1c. The lower PVR in the measured  $I(V_b)$  compared with those in our calculations may arise in part from small leakage currents between the graphene electrodes involving other tunnelling mechanisms or a more complex  $V_S(q)$  with less sharp cutoff than assumed in our model. Our analysis also explains the origin of the shoulder-like feature beyond the resonant peak in reverse bias: the shoulder occurs when  $V_b$  and  $V_g$  correspond to the alignment of the chemical potential in the top graphene layer with the Dirac point of the bottom layer. When this condition is satisfied, the carriers close to the Fermi energy in one electrode tunnel into a very low density of states in the other, so that the measured current is insensitive to small changes of  $V_b$ , thus yielding a differential conductance close to zero.

**Resonant tunnelling and NDC at room temperature.** Figure 3 showing data for another transistor, device B, illustrates the reproducibility of the I-V characteristics for different devices and the persistence of the resonant tunnelling effect up to room temperature, a key property for future device applications. In this device, a PVR of up to  $\approx 4$  is obtained at low  $T$  (see inset of Fig. 3a) and the resonant peak and NDC remain clearly defined at room temperature (Fig. 3b). The dependence of the PVR on  $V_g$  (inset of Fig. 3a) is qualitatively similar to device A and closely reproduces that obtained from the model (bottom right inset of Fig. 1c).



**Figure 2 | Idealized current-voltage characteristics of a resonant tunnel transistor.** Here, we assume that the chemical potentials of the two graphene electrodes are at the Dirac points when the device is unbiased.  $T = 10$  K.  $V_g = 0$  (black curve);  $V_g = 10$  V (red curve). Insets (a–d) show the positions of the chemical potentials at the marked points on the  $I(V_b)$  curves.



**Figure 3 | Reproducibility of resonant tunnelling in double-layer graphene devices.** Device B exhibits  $I(V_b)$  curves similar to those of device A. The hBN barrier is 5 atomic layers thick; the active area for the flow of tunnel current is  $0.6 \mu\text{m}^2$ . **(a)**  $T = 7 \text{ K}$ ; the  $V_g$  values range, in 5 V steps, from +20 to -60 V. The inset shows the  $V_g$  dependence of the PVR. **(b)** Room-temperature  $I(V_b)$  characteristics for device B;  $V_g$  ranges from +50 to -50 V in 5 V steps.

## Discussion

Several different mechanisms by which NDC can be generated in graphene-based devices have been modelled theoretically, for example, refs 3,18,27. The observation of NDC in a graphene field effect tunnel transistor in which the current flows along the graphene layer was also reported recently. In this device, a tunnel barrier potential is formed in the plane by applying a gate voltage across a silicon nitride dielectric stripe deposited on a single graphene layer<sup>37</sup>. Our device, in which the tunnel current flows perpendicular to the plane of the component layers, compares very favourably with the planar device, particularly with regard to its strong NDC and high PVR. It is also interesting to compare our device with resonant tunnelling in double barrier devices made from conventional semiconductor heterostructures<sup>38,39</sup>. In those devices, the quantum well confinement provided by the two potential barriers creates quasi-two-dimensional states through which charged carriers can tunnel when their energy is tuned to resonance by an applied voltage. In contrast, our devices consist of a single-tunnel barrier, so the device speed is not limited by the dwell time of the carriers in a central quantum well<sup>40,41</sup>. Although the PVR of our proof-of-concept devices is significantly lower than that achieved in state-of-the-art III-V double barrier resonant tunnelling diodes<sup>42,43</sup>, there are good prospects of achieving higher PVRs. In addition, as the barrier transmission coefficient is exponentially sensitive to the number of atomic layers in the hBN barrier<sup>13</sup>, it should be possible to achieve much higher peak resonant current densities in devices by using, for example, three-monolayer barriers.

We note the recent theoretical work by Feenstra *et al.*<sup>15,26</sup>, which modelled carrier tunnelling in multilayer graphene-dielectric-graphene tunnel diodes. That work considered how crystal grain size and spatial misorientation of the lattices of the two graphene electrodes can influence resonant tunnelling. Microstructural analysis<sup>2,12,13</sup> of the graphene and boron nitride layers that make up our devices indicates that they have a high level of structural perfection, so grain size effects are unlikely to have a major influence on the behaviour of our devices. Supplementary Note 1 discusses how we incorporate the effects of misorientation of the graphene lattices in our model of the device characteristics.

In summary, we have shown how to achieve gate-controlled resonant tunnelling with high PVR and pronounced NDC in graphene-based multilayer, 'vertical' transistors. These devices could be developed further for applications in logic circuits that

exploit the multi-valued form of the current-voltage characteristics. The additional functionality provided by resonant tunnelling is not available in graphene 'barristors'<sup>23</sup> in which the current flow arises from carriers that are thermally activated over a Schottky potential barrier. Furthermore, one of the key factors that limits the speed of conventional double barrier resonant tunnelling diodes, namely the dwell time of carriers in the central quantum well at resonance, is avoided in our proof-of-concept device architecture. This, combined with the high mobility of the carriers in the graphene electrodes and the atomically thin tunnel barrier, suggests potential applications in high-speed electronics.

## Methods

**Device fabrication.** The methods used for fabricating this type of the device are given in refs 12 (and its supporting online material) and ref. 13.

**Measurement.** The measurements of the current-voltage characteristics of the devices were made using Keithley Model 2400 voltage sources to apply the bias voltage between the two graphene electrodes and to apply the gate voltage between the lower graphene electrode and the doped silicon substrate, which acted as the gate electrode. The current flowing between the electrodes was recorded by using a Keithley 2182A nanovoltmeter to measure the voltage drop across a known resistance. The device was mounted on a ceramic chip carrier and placed on a sample holder inserted into an Oxford Instruments variable temperature cryostat for the low-temperature measurements. The room temperature measurements were made either in the same insert or in ambient conditions with the sample mounted in a screened box. All external electrical connections were made using standard coaxial cables via a breakout box.

**Theoretical model.** The theoretical model used to fit our data is described in Supplementary Note 1.

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## Author contributions

A.K.G., K.S.N. and L.E. conceived and designed the experiments, which were performed by L.B., R.V.G., L.A.P. and A.M. A.K.G., M.T.G., T.M.F., K.S.N. and L.E. analysed the data; M.T.G., T.M.F. and L.E. wrote the Supplementary Information and developed the model. M.T.G. wrote code and ran the model. The Letter was written by A.K.G., T.M.F. and L.E. with contributions from all authors.

## Additional information

**Supplementary Information** accompanies this paper at <http://www.nature.com/naturecommunications>

**Competing financial interests:** The authors declare no competing financial interests.

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