transistors on a single chip–enough for several GRAPE processors.

But semiconductor technology cannot be pushed that much further — certainly not by several orders of magnitude. Feature sizes are limited by quantum physics, and clock frequencies approaching 1 GHz correspond to cycle times of a few nanoseconds: electrical signals travel less than a metre in this time, posing serious design problems for computers of any physical size. The continual pursuit of ever greater computer performance will inevitably lead to new technologies being developed.

Recent advances in nonlinear optical materials and devices, largely driven by the rapid uptake of optics in telecommunications, have brought us to the threshold of the integration of optics with electronics in computing. One word sums up what optics means to computing — parallelism. Large numbers of light beams can cross the same region of space without interfering, and signals of different wavelengths can be sent simultaneously along the same path. Groups in Europe, Japan and the United States are developing algorithms, architectures and devices for both optoelectronic and all-optical computers. In the last few months, systems that can reasonably claim to be digital optical computers have been demonstrated independently at AT&T Bell Laboratories in the United States[3] and Heriot–Watt University, Edinburgh, in the UK[4]. A colleague and I have recently designed an application-specific optoelectronic computer which would process images at the speed of one million Vaxes, using the fundamental operations of binary image algebra as its instruction set. Its feasibility has been verified by simulations on a 'conventional' electronic parallel computer, and such a computer can be developed to perform more general array processing[5]. The technology will exist to build this machine, and others like it, within the next three years: for example, it has been recognized for more than two decades that optics might provide the very large number of connections needed for neural networks, and a variety of proposals for optical neural computers are now being seriously pursued.

A problem with any hardware solution such as a GRAPE chip[1], is that it is extremely costly to debug: almost any error in design or implementation means re-engineering, in expensive contrast to editing an erroneous line of software. The technologies for programmable parallel computers are rapidly maturing, and can deliver gigaflop performance. Typical systems use reconfigurable arrays of off-the-shelf microprocessors, interconnected by switchable routing chips which are software-controlled. Such systems often have better cost/performance than either dedicated hardware or supercomputers, and enormously extend the realm of software solutions.

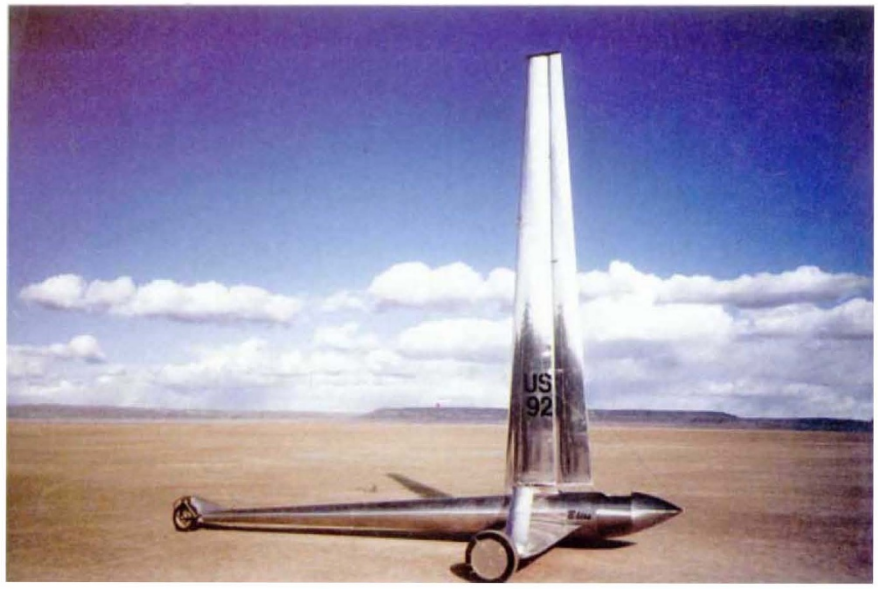
A promising new technology which blurs the distinction between hardware and software is configurable array logic, based on a model, such as a cellular automaton, rather than an instruction set. Implemented as an electronically reconfigurable array (a kind of generic integrated circuit, parts of which can be electrically modified after manufacture), 'programming' is a very low-level task, achieved by physically editing the content of control registers — not dissimilar to machine-code programming of microprocessors. The particular model implemented limits the uses of such a device, but, unlike conventional integrated circuits, debugging does not involve throwing them away and making new ones.

Special-purpose hardware like that proposed by Sugimoto *et al.* is neither inferior nor superior to either general-purpose computers, or reconfigurable parallel computers or any other solution. Each approach trades ease of implementation and general applicability for cost/performance in different ways. The excitement of advances in both hardware and software solutions is that it is now becoming possible to tackle problems never previously attempted, not because we did not know how, but because they were not computationally feasible. □

Colin Upstill is at Plessey Research, Roke Manor, Romsey, SO51 0ZN, UK.

1. Sugimoto, D. *et al. Nature* **345**, 33–35 (1990).
2. Hut, P., Makino, J. & McMillan, S.L.W. *Nature* **336**, 31–35 (1988).
3. Prise, M.E. *et al. Proc. 1990 Int. Topical Meet. Optical Computing* 122–123 (The Japan Society of Applied Physics, Tokyo, 1990).
4. Wherrett, B.S. *et al. Proc. 1990 Int. Topical Meet. Optical Computing*, 154–159 (The Japan Society of Applied Physics, Tokyo, 1990).
5. Cramb, I. & Upstill, C. *Proc. 1990 Int. Topical Meet. Optical Computing* 130–131 (The Japan Society of Applied Physics, Tokyo, 1990).

Land yacht earns its wings



THIS winged "land yacht", designed by two Oregon inventors and the US National Aeronautics and Space Administration (NASA), finished second in the world last month at the World Cup Regatta international land sailing championship.

Inspired by the vertical-wing design of *Stars and Stripes*, the US catamaran that soundly defeated New Zealand in last year America's Cup race, the yacht uses a NASA-designed laminar-flow airfoil to reach speeds of nearly 90 m.p.h. in a 20 m.p.h. wind. Amateur inventors Philip and Art Rothrock collaborated on the project with engineer Harry Morgan of the Langley Research Station's Subsonic Aerodynamics Branch, incorporating three decades of NASA research on low-drag aerodynamics.

With a laminar-flow airfoil, the boundary layer of moving air closest to the surface of the wing stays smooth and non-chaotic until it approaches the rear of the airfoil, much further back than in traditional airfoil designs. Because drag is proportional to the amount of wing surface over which airflow has become turbulent, laminar-flow wings typically demonstrate drag reductions of 30 per cent or more over traditional designs.

Because only the high end of the land yacht's performance falls within NASA's test data for low-speed, high-lift airfoils, much of the vehicle's final design has been worked out during trials on desert or dry-lake test courses.

G. Christopher Anderson