Supplementary Figures

Supplementary Figure S1 | Schematic of the fabrication process of G/SiO$_x$/ITO devices.
Supplementary Figure S2 | Electroforming process in a G/SiO$_x$/ITO device. The numbers near the $I$-$V$ curves indicate the corresponding sweep orders. The device was initially in a non-conduction state. By a voltage sweep to a high value (e.g., +40 V, green curve), a sudden current increase (to $\sim 10^{-6}$ A) was induced at $\sim 33$ V, accompanied by current fluctuations. During the subsequent voltage sweeps (curves 2 and 3), the currents gradually increased, as did the current fluctuations. And a characteristic resistive switching $I$-$V$ (black curve) then appeared, featuring the sudden current increase and drop defining the set and reset values, respectively. The arrows indicate the voltage sweep directions. This electroforming process is similar to those described in SiO$_x$-based resistive switching systems$^{17,20}$. 
Supplementary Figure S3 | SEM characterizations. Left panel shows a SEM images of the G/SiO\textsubscript{x}/ITO devices as described in Fig. 1 in the main article and the right panel shows the control SiO\textsubscript{x}/ITO devices without the top graphene layers. Scale bars, 100 µm. Over 20 devices were randomly selected for each type of the structures for the electrical characterizations. 70% of the G/SiO\textsubscript{x}/ITO devices tested showed memory switching properties as described in the main article. No switching was observed by directly landing of the probe-tip on the SiO\textsubscript{x} layer in the control SiO\textsubscript{x}/ITO devices. The the right panel inset shows an enlarged picture of the SiO\textsubscript{x}-layer surface, showing uniform morphology without surface pinholes; scale bar, 10 µm. Together, they ruled out the possibility of metal-filament switching caused by the probe tip in contact with the top electrode and further indicated the edge-localized switching\textsuperscript{17}. 

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Supplementary Figure S4: Distribution of $V_{\text{set}}$ and ON/OFF ratio. Statistics of (a) $V_{\text{set}}$ and (b) $I_{\text{on}}, I_{\text{off}}$ in G/SiO$_x$/ITO devices. The $I_{\text{on}}$ and $I_{\text{off}}$ states were read at +1 V.
Supplementary Figure S5 | Schematic of the fabrication process of G/SiO$_x$/G devices.
Supplementary Figure S6 | G/SiOx/G pillar structures on plastic substrate. (a) Characteristic resistive switching I-V curve from a G/SiOx/G pillar structure on the plastic substrate. The arrows indicate the voltage-sweep directions and the numbers indicate the order. (b) Retention of both ON (green curve) and OFF (blue curve) memory states (read at +1 V) from a G/SiOx/G pillar structure is shown upon bending the plastic substrate around a ~1.2-cm diameter curvature.
Supplementary Figure S7 | Formation of the nanogap and the subsequent electroforming process in planar graphene device. The fabrication of the graphene devices are described in the main letter. The as-made graphene device initially showed metallic transport property. The conduction suddenly dropped when the voltage reached to certain value (e.g., ~ 18 V), indicated by the black arrow in (a). Correspondingly, a disruption region or nanogap\textsuperscript{19} in the graphene stripe was formed (bottom panel in Fig. 5b). (b). During the subsequent voltage sweep, the current level suddenly jumped at ~ 10 V (indicated by the black arrow), featuring the beginning of the soft breakdown in the SiO\textsubscript{x} at the nanogap region. Further voltage sweeps increased the current levels (accompanied with fluctuations), featuring the typical electroforming process as described in Fig. S2, until at last the characteristic resistive switching $I-V$ curve was formed (blue curve). The numbers beside the $I-V$ curves indicate the voltage-sweep order.
Supplementary Figure S8 | Analogy between a backward voltage sweep and the falling edge in a pulse. (a). Schematic of a backward voltage sweep starting from the reset region bypasses the set region at a slow sweep rate (red curve) and the corresponding current (blue curve). (b) Schematic of the falling edge (red line) in a reset pulse.
Supplementary Discussion

As the set and reset processes are largely field-driven and thermal-driven, respectively, the mechanistic switching scenario is as follows: at $V > V_{\text{set}}$, the electric field is always sufficient to set the device ON; at $V \geq V_{\text{reset}}$, the thermal effect (reset) begins to override the field effect (set). Note that although the $I$-$V$ curve in the reset region ($V \geq V_{\text{reset}}$) appears to be at a static high-resistance state, it indeed involves a dynamic competing process with the thermal effect constantly overriding the field effect to prevent the set process (the larger current fluctuation in this region as shown in Fig. 1b is an indication). The thermal effect can no longer override the field effect at $V_{\text{set}} < V < V_{\text{reset}}$, and the state returns to a low-resistance one in the backward sweep.

The falling edge in a reset pulse (b) is analogous to the backward voltage sweep in (a), but it does not incur the set process. The possible reason is that the falling edge in the pulse (~10 ns) is much faster than the $I$-$V$ sweep (~3 V/s). Since the set process was tested to be fast in the pulse mode (e.g., < 1 µs), it may indicate that the falling edge needs to be faster than this in the reset pulse. Meanwhile, we also acknowledge the difference: during the falling edge in a reset pulse, the device is in a “hot” state since the voltage starts from the reset region, as opposed to a “cool” state in the set operation. This “hot” state may prevent the set process incurred during the falling edge. The detailed study of this aspect has not yet been done.