**Figure 1. Flowchart for assessing performance of FETs**

Flowchart for evaluating the key parameters of a ballistic FET consisting of a 2D channel, shown schematically in the lower left corner (G = gate, S = source, D = drain, blue region is the gate dielectric). The application of a gate bias $V_{gs}$ introduces a gate capacitance ($C_b$), which in turn results characteristic carrier density in the channel ($n_b$) above the threshold voltage. The tuning of the carrier concentration via modulation of gate voltage results in an expression that relates the mobile carrier density $n_s(V_{gs})$ in the semiconductor channel as a function of the gate voltage $V_{gs}$ [equation (4)], which includes the 2D carrier concentration ($n_q$) term that is related to the density of states at the band edge of the 2D semiconductor ($D_0$). The influence of the drain voltage, $V_{ds}$, on the can be obtained from the dimensionless degeneracy source term ($\eta_s$). From the gate and drain electrostatics, it is possible to extract the FET operation characteristics in terms of the drain current with gate voltage from the equation shown in the bottom right corner.